UNISTAR-IOP

NORMAL k DESIGNATOR

k	READ		STORE		REPLACE			JUMP	
	MN.	Origin	MN.	Dest.	MN.	Origin	Dest.	MN.	Jump to Modulo 2^{18}
0	'blank'	sy + Bb	QR	Q	'not used'	--	--	'blank'	sy + Bb
1	L	Y_L	L	Y_L	L	Y_L	Y_L	L	Y_L
2	U	Y_U	U	Y_U	U	Y_U	Y_U	U	Y_U
3	W	Y	W	Y	W	Y	Y	W	Y
4	RX	X[sy] + Bb	AS	A	'not used'	--	--	RX	Ys + Bb
5	LX	XY_L	CPL	$Y_L' \rightarrow Y_L$	LX	XY_L	Y_L	LX	XY_L
6	UX	XY_U	CPU	$Y_U' \rightarrow Y_U$	UX	XY_U	Y_U	UX	XY_U
7	AR	A	CPW	$Y' \rightarrow Y$	'not used'	--	--	AR	(A)

Y = (Ys + Bb)
Ys = Selected SR (4-0) or P (17-13) concatenated with y (12-0)
sy = s (14-13) concatenated with y (12-0)
W = Whole word

L = Lower half
U = Upper half
X = Sign extention
CP = Complement
MN = Mnemonic

SPECIAL $\hat{j}$ DESIGNATOR

$\hat{j}$	C f04	M f22 k≠7	D f23 k≠7	LLP f40	RLP f44	AQ f26	ANQ f27
0	0: No Skip	0: No Skip	No Skip	0: No Skip		0; No Skip	
1	SK: Skip	SK: Skip	Skip	SK: Skip		SK: Skip	
2	YLEQ: Y ≤ (Q)	NOVF: $Q_{29} = A_{29}$	No Over flow	EVEN: Even Parity		AP: A Positive	
3	YGTQ: Y > (Q)	OVF: $Q_{29} \neq A_{29}$	Over flow	ODD: Odd Parity		AN: A Negative	
4	YIN: (A) < Y ≤ (Q)	AZ: A = ±Zero	A = ±Zero	AZ: A + Zero		QZ: Q + Zero	
5	YOUT: Y > (Q) or Y ≤ (A)	ANZ: A ≠ ±Zero	A ≠ ±Zero	ANZ: A Not + Zero		QNZ: Q Not + Zero	
6	YLEA: Y ≤ (A)	6: Skip	Skip	AP: A Positive		QP: Q Positive	
7	YGTA: Y > (A)	7: No Skip	No Skip	AN: A Negative		QN: Q Negative	

The IOP interprets the "s" designator for the following instructions:
For all Format I read instructions 01-13, 20-23, 26-31, 40, 43, 50-52, 71 when k ≠ 0, 4, 7.
For all Format I store instructions 14-16, when k ≠ 0, 4.
For all replace instructions 24, 25, 34-37, 44, 54-56 when k ≠ 0, 4, 7.
For instructions 17, 62, 63, 67, 74-76 with all k values.
For instructions 7705, 7726, 7727.
For instructions 7742, 7745, 7760, 7770 when $\hat{j} \neq 0$.
For jump instructions, 60, 61, 65, 72, 73 when k ≠ 0, 7.

NORMAL b DESIGNATOR

b	MNEMONIC	DESCRIPTION
0	'blank'	No Mod
1	B1	B1
2	B2	B2
3	B3	B3
4	B4	B4
5	B5	B5
6	B6	B6
7	B7	B7

NORMAL j DESIGNATOR

j	MNEMONIC	DESCRIPTION
0	'blank'	No Skip
1	SK	Skip
2	QP	Skip if Q Positive
3	QN	Skip if Q Negative
4	AZ	Skip if A + Zero
5	ANZ	Skip if A Not + Zero
6	AP	Skip if A Positive
7	AN	Skip if A Negative

ADDRESS EXTENSION(s) DESIGNATOR

s	MNEMONIC	DESCRIPTION
00	S0	SR0
01	S1	SR1
10	S2	SR2
11	S3 or 'blank'	Bit 17-13 of P

SPECIAL d,e,c DESIGNATOR

DES	MNEMONIC	DESCRIPTION
d	ND	Normal Device Interrupts
e	EIS	External Interrupt & Status Words
c	CI	Channel Interrupts (Class V)

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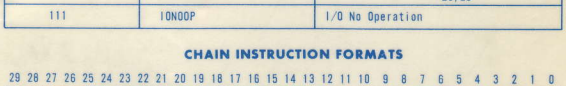
UNISTAR*IOP

CHAIN INSTRUCTIONS

BINARY FUNCTION CODE	SYMBOLIC CODE SEQUENCE(S)		DESCRIPTION
00	BCW	n,y	Buffer Control Word, n=number of words to be transferred
010 j=0,k=0	EFW	y,I	External Function: Whole Word, I=1 for Indirect
010 j=1,k=0	FEFW	y,I	Force External Function: Whole Word, I=1 for Indirect
010 j=0,k=1	EFH	y,I	External Function: Half Word, I=1 for Indirect
010 j=1,k=1	FEFH	y,I	Force External Function: Half Word, I=1 for Indirect
011	IOSTOP,m		I/O Stop, m=1 for Monitor Interrupt
100	IOCL	y	I/O Clear Flag: $0 \rightarrow (y_{29,28})$
101	IOJ,m,k	y	I/O Jump, m=1 for Monitor Interrupt, k=1 insert channel number in y_{3-0}
110	IOSET	y	I/O Set Flag: $1 \rightarrow (y_{29,28})$
111	IONOOP		I/O No Operation

CHAIN INSTRUCTION FORMATS



INTERRUPTS

INTERRUPT BY PRIORITY ①	INDIVIDUAL CLASS INTERRUPTS	RELATIVE INTERRUPT ENTRANCE ADDRESS (BINARY) ②
Power Class I (highest)	Power Tolerance Error	1 00X XX0 010
Hardware Class II (first come – first served priority)	Memory Address Parity Error Memory Resume Error Memory Data Parity Error	1 011 000 000
	High Priority Device Interrupt (a memory resume interrupt occurs if this address is non-existent)	100 001 00X XX1 001
Program Class III	Program Fault Monitor Clock	1 011 000 001 1 00X XX1 010
Normal Communication Class IV	Normal Device Interrupt	1 00X XX1 001
Class V	I/O Channel Interrupt	0 XXX CCC C11

NOTES: ① If AUTO START switch is selected and power applied, processor starts at address 1 00X XX0 001.
② XXX implies 3 bit device number placed in address, thus completing relative address. CCCC represents channel number.

UNISTAR IOP

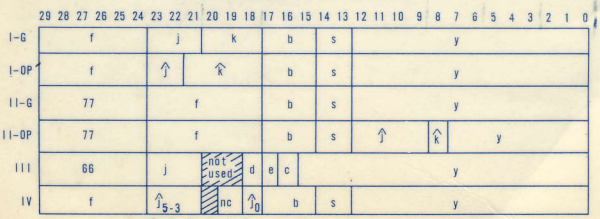
REPERTOIRE OF INSTRUCTIONS

FUNCTION CODE	FORMAT	SYMBOLIC CODE SEQUENCE(S)		DESCRIPTION
01	I-G	SRQ, j	y,k,b,s	Shift Right (Q) by Y
02	I-G	SRA, j	y,k,b,s	Shift Right (A) by Y
03	I-G	DSR, j	y,k,b,s	Double Shift Right (AQ) by Y
04 ①	I-G	C, $\hat{j}$	y,k,b,s	Compare Y with A, Q or A & Q
05	I-G	SLQ, j	y,k,b,s	Shift Left (Q) by Y
06	I-G	SLA, j	y,k,b,s	Shift Left (A) by Y
07	I-G	DSL, j	y,k,b,s	Double Shift Left (AQ) by Y
10	I-G	LQ, j	y,k,b,s	Load Q: Y → Q
10 y=k=0	I-G	ZQ, j		Clear Q: 0 → Q
11	I-G	LA, j	y,k,b,s	Load A: Y → A
11 y=k=0	I-G	ZA, j		Clear A: 0 → A
12	I-G	LB	j,y,k,b,s	Load Bj: Y → Bj
12 y=k=0	I-G	ZB	j	Clear Bj: 0 → Bj
12 j=0	I-G	NOOP		No Operation
13	I-G	ENY	j,y,k,b,s	Encode Y: Y (encoded) → Bj
14	I-G	SQ, j	y,k,b,s	Store Q: (Q) → Y
14 k=0	I-G	CPQ, j		Complement Q: (Q)' → Q
15	I-G	SA, j	y,k,b,s	Store A: (A) → Y
15 k=4	I-G	CPA, j		Complement A: (A)' → A
16	I-G	SB	j,y,k,b,s	Store Bj: (Bj) → Y
16 j=0	I-G	SZ	y,k,b,s	Store Zero: 0 → Y
17 k=0	I-G	STIME	j	Select Timing Source: j = Device Number
17 k=1	I-G	NINT	j	Normal Priority Interrupt: j = Device Number
17 k=2	I-G	HINT	j	High Priority Interrupt: j = Device Number
20	I-G	AA, j	y,k,b,s	Add to A: (A) + Y → A
21	I-G	ANA, j	y,k,b,s	Add Negative to A: (A) − Y → A
22 k≠7 ①	I-G	M, $\hat{j}$	y,k,b,s	Multiply: (Q) · Y → AQ
23 k≠7 ①	I-G	D, $\hat{j}$	y,k,b,s	Divide: (AQ) ÷ Y → Q; remainder → A
24	I-G	RA, j	y,k,b,s	Replace Add: (A) + Y → Y & A
25	I-G	RAN, j	y,k,b,s	Replace Add Negative to A: (A) − Y → Y & A
26 ①	I-G	AQ, $\hat{j}$	y,k,b,s	Add to Q: (Q) + Y → Q
27 ①	I-G	ANQ, $\hat{j}$	y,k,b,s	Add Negative to Q: (Q) − Y → Q
30	I-G	LSUM, j	y,k,b,s	Load Sum: Y + (Q) → A
31	I-G	LDIF, j	y,k,b,s	Load Difference: Y − (Q) → A
34	I-G	RSUM, j	y,k,b,s	Replace Sum: Y + (Q) → Y & A
35	I-G	RDIF, j	y,k,b,s	Replace Difference: Y − (Q) → Y & A
36	I-G	RI, j	y,k,b,s	Replace Increment: Y + 1 → Y & A
37	I-G	RD, j	y,k,b,s	Replace Decrement: Y − 1 → Y & A
40 ①	I-G	LLP, $\hat{j}$	y,k,b,s	Load Logical Product: L [Y(Q)] → A
43 ①	I-G	CM, j	y,k,b,s	Compare Mask: (A) − L [Y(Q)] → A sense j, (A) + L [Y(Q)] → A
44 ①	I-G	RLP, $\hat{j}$	y,k,b,s	Replace Logical Product: L [Y(Q)] → Y & A
50	I-G	OR, j	y,k,b,s	Inclusive OR: Set $(A)_n$ for $Y_n = 1$
51	I-G	XOR, j	y,k,b,s	Exclusive OR: Complement $(A)_n$ for $Y_n = 1$
52 k≠7	I-G	SC, j	y,k,b,s	Selective Clear: Clear $(A)_n$ for $Y_n = 1$
54	I-G	ROR, j	y,k,b,s	Replace OR: [Set $(A)_n$ for $Y_n = 1$] → Y & A
55	I-G	RXOR, j	y,k,b,s	Replace Exclusive OR: [CPL $(A)_n$ for $Y_n = 1$] → Y & A
56	I-G	RSC, j	y,k,b,s	Replace Selective Clear: [Clear $(A)_n$ for $Y_n = 1$] → Y & A
60 j=0	I-G	RIL		Remove Class V Interrupt Lockout
60 j=1	I-G	JRIL	y,k,b,s	Jump and Remove Class V Interrupt Lockout
60 j=2	I-G	JQP	y,k,b,s	Jump if Q Positive
60 j=3	I-G	JQN	y,k,b,s	Jump if Q Negative
60 j=4	I-G	JAZ	y,k,b,s	Jump if A + Zero

① See List of Special $\hat{j}$ Designators

All non-existent function codes will cause control to be transferred to the program fault interrupt entrance address.

INSTRUCTION WORD FORMATS



UNISTAR IOP

REPERTOIRE OF INSTRUCTIONS

FUNCTION CODE	FORMAT	SYMBOLIC CODE SEQUENCE(S)		DESCRIPTION
60 j=5	I-G	JANZ	y,k,b,s	Jump if A not + Zero
60 j=6	I-G	JAP	y,k,b,s	Jump if A Positive
60 j=7	I-G	JAN	y,k,b,s	Jump if A Negative
61 j=0	I-G	J	y,k,b,s	Jump
61 j=1-7	I-G	JC, j	y,k,b,s	Jump Conditional if Jump j is selected
61 j=4-7	I-G	JSC, j	y,k,b,s	Stop Conditional if Stop j selected and Jump on Restart
62 $\hat{j}$=0	I-OP	ICIN	$\hat{k}$,y,b,s	Load/Initiate Chain Input: $\hat{k}$ = 4 Bit Channel Number
62 $\hat{j}$=1	I-OP	ICOUT	$\hat{k}$,y,b,s	Load/Initiate Chain Output: $\hat{k}$ = 4 Bit Channel Number
62 $\hat{j}$=2	I-OP	IBIN	$\hat{k}$,y,b,s	Initiate Input or EF Buffer: $\hat{k}$ = 4 Bit Channel Number
62 $\hat{j}$=3	I-OP	IBOUT	$\hat{k}$,y,b,s	Initiate Output or EF Buffer: $\hat{k}$ = 4 Bit Channel Number
63 $\hat{j}$=0	I-OP	LCIN	$\hat{k}$,y,b,s	Load Input Chain Pointer: $\hat{k}$ = 4 Bit Channel Number
63 $\hat{j}$=1	I-OP	LCOUT	$\hat{k}$,y,b,s	Load Output Chain Pointer: $\hat{k}$ = 4 Bit Channel Number
63 $\hat{j}$=2	I-OP	LBIN	$\hat{k}$,y,b,s	Load Input BCW: $\hat{k}$ = 4 Bit Channel Number
63 $\hat{j}$=3	I-OP	LBOUT	$\hat{k}$,y,b,s	Load Output BCW: $\hat{k}$ = 4 Bit Channel Number
65 j=0	I-G	RJ	y,k,b,s	Return Jump
65 j=1-7	I-G	RJC, j	y,k,b,s	Return Jump Conditional if Jump j selected:
65 j=4-7	I-G	RJSC, j	y,k,b,s	Stop if Stop j Selected and Return Jump on Restart
66 j=0	III	STOP		Unconditional Stop
66 j=1	III	TIO	y	Terminate I/O on Channel n for $y_n = 1$
66 j=2 ②	III	SIL,d,e,c	y	Disable Interrupts on Channel n for $y_n = 1$
66 j=3 ②	III	RIL,d,e,c	y	Enable Interrupts on Channel n for $y_n = 1$
67 $\hat{j}$=0	I-OP	SCIN	$\hat{k}$,y,b,s	Store Chain Input Pointer: $\hat{k}$ = 4 Bit Channel Number
67 $\hat{j}$=1	I-OP	SCOUT	$\hat{k}$,y,b,s	Store Chain Output Pointer: $\hat{k}$ = 4 Bit Channel Number
67 $\hat{j}$=2	I-OP	SBIN	$\hat{k}$,y,b,s	Store Input BCW: $\hat{k}$ = 4 Bit Channel Number
67 $\hat{j}$=3	I-OP	SBOUT	$\hat{k}$,y,b,s	Store Output BCW: $\hat{k}$ = 4 Bit Channel Number
71	I-G	BSK	j,y,k,b,s	(Bj) = Y, Skip NI and Clear (Bj);(Bj) ≠ Y, advance Bj
72 j=0	I-G	CPFI		Clear Program Fault Indicator
72 j≠0	I-G	JBNZ	j,y,k,b,s	(Bj) = 0 Read NI; (Bj) ≠ 0,(Bj) − 1 → Bj & Jump to Y
73 j=0	I-G	JOVF	y,k,b,s	Jump if Overflow Bit Set
73 j≠0	I-G	LBJ	j,y,k,b,s	Load Bj and Jump
74 ③	IV	PULLT	$\hat{j}$,y,b,s	If Table Not Empty, Pull Top and Skip NI
75 ③	IV	PULLB,nc	$\hat{j}$,y,b,s	If Table Not Empty, Pull Bottom and Skip NI
76 ③	IV	PUSHT,nc	$\hat{j}$,y,b,s	If Table Not Full, Push Top and Skip NI
7705	II-G	XR	y,b,s	Execute Remote: Read NI from Y
7726	II-G	LMC	y,b,s	Load and Enable Monitor Clock: Y → Monitor Clock
7727	II-G	TSF	y,b,s	Test and Set Flag: If $Y_{29,28}$=0, Skip NI & Set $Y_{29,28}$: If $Y_{29,28} \neq 0$, Do NI
7742 $\hat{k}$=1	II-OP	LST	y,b,s	Load Status Register: Y → Status Reg.
7745 $\hat{k}$=1	II-OP	SST	y,b,s	Store Status Register: (Status Reg.) → Y
7745 $\hat{k}$=0	II-OP	SSTQ		Store Status Register: (Status Reg.) → Q
7760	II-OP	LSR	$\hat{j}$,y,$\hat{k}$,b,s	Load Address Extension Register ($SR\hat{j}$, j = 0,1,2) with: $\hat{k}$=0: $Y_{4-0} \rightarrow SR\hat{j}$ $\hat{k}$=1: $(Y)_{4-0} \rightarrow SR\hat{j}$
7770	II-OP	SSR	$\hat{j}$,y,$\hat{k}$,b,s	Store Address Extension Register ($SR\hat{j}$, j=0,1,2) with: $\hat{k}$=0: $SR\hat{j} \rightarrow Q_{4-0}$ and Clear Q_{29-5} $\hat{k}$=1: $SR\hat{j} \rightarrow Y_{4-0}$ and Clear Y_{14-5}

② See List of Special d,e,c, Designators

③ See List of Special Push, Pull $\hat{j}$ Designators. nc = Non-Circular (Opt.) Otherwise Circular

Y = The Operand Regardless of Source, i.e., y, (Y), Y or sy

Y = The Source or Destination of the Operand, i.e., y extended plus Bb

PUSH, PULL CONTROL PARAMETER WORDS

	29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Y	TOP SPACE COUNT (TSC)	TOP ADDRESS POINTER (TAP)
Y + 1	BOTTOM SPACE COUNT (BSC)	BOTTOM ADDRESS POINTER (BAP)
Y + 2	LIST LENGTH (LL)	BASE ADDRESS (BA)

SPECIAL PUSH, PULL $\hat{j}$ DESIGNATORS

$\hat{j}_{5-3}$	$\hat{j}_0$:0	$\hat{j}_0$:1
0	RTC	SO : SR0
1	B1	S1 : SR1
2	B2	S2 : SR2
3	B3	AR : A Reg.

$\hat{j}_{5-3}$	$\hat{j}_0$:0	$\hat{j}_0$:1
4	B4	QR : Q Reg.
5	B5	SR : Status Reg.
6	B6	UNDEFINED
7	B7	UNDEFINED