REPERTOIRE OF INSTRUCTIONS

FUNCTION CODE	NOTES*	FORMAT	SYMBOLIC CODE SEQUENCE(S)	DESCRIPTION
01		I-G	SRQ,j y,k,b,s	Shift Right (Q) by Y
02		I-G	SRA,j y,k,b,s	Shift Right (A) by Y
03		I-G	DSR,j y,k,b,s	Double Shift Right (AQ) by Y
04	1	I-G	C,j y,k,b,s	Compare Y with A, Q or A & Q
05		I-G	SLQ,j y,k,b,s	Shift Left (Q) by Y
06		I-G	SLA,j y,k,b,s	Shift Left (A) by Y
07		I-G	DSL,j y,k,b,s	Double Shift Left (AQ) by Y
10		I-G	LQ,j y,k,b,s	Load Q: Y → Q
10 y=k=0		I-G	ZQ,j	Clear Q: 0 → Q
11		I-G	LA,j y,k,b,s	Load A: Y → A
11 y=k=0		I-G	ZA,j	Clear A: 0 → A
12		I-G	LB j,y,k,b,s	Load Bj: Y → Bj
12 y=k=0		I-G	ZB j	Clear Bj: 0 → Bj
12 j=0		I-G	NOOP	No Operation
13		I-G	ENY j,y,k,b,s	Encode Y: Y (encoded) → Bj
14 k≠0		I-G	SQ, j y,k,b,s	Store Q: (Q) → Y
14 k=0		I-G	CPQ, j	Complement Q: (Q)' → Q
15 k≠4		I-G	SA, j y,k,b,s	Store A: (A) → Y
15 k=4		I-G	CPA,j	Complement A: (A)' → A
16		I-G	SB j,y,k,b,s	Store Bj: (Bj) → Y
16 j=0		I-G	SZ y,k,b,s	Store Zero: 0 → Y
17 k=0		I-G	STIME j	Select Timing Source: j = Device Number
17 k=1	2	I-G	NINT j,y,b,s	Normal Priority Interrupt: j = Device Number
17 k=2	2, 9	I-G	HINT j,y,b,s	High Priority Interrupt: j = Device Number
17 k=4	5	I-G	NDROD	NDRO Disable: Clear NDRO Enable F/F
17 k=5	5	I-G	NDROE	NDRO Enable: Set NDRO Enable F/F
17 k=6	5	I-G	IPSS j	Interprocessor Stop: Signal → Processor j
17 k=7	5	I-G	SCATI	Catchet Interrupt: Cause Interrupt to all Processors
20		I-G	AA,j y,k,b,s	Add to A: (A) + Y → A
21		I-G	ANA,j y,k,b,s	Add Negative to A: (A) − Y → A
22 k≠7	1	I-G	M,j y,k,b,s	Multiply: (Q) · Y → AQ
23 k≠7	1	I-G	D,j y,k,b,s	Divide: (AQ) ÷ Y → Q: Remainder → A
23 k=7	6	I-G	RT,j	Square Root: √(Q) → Q: Remainder → A; Overflow Impossible
24		I-G	RA,j y,k,b,s	Replace Add: (A) + Y → Y & A
25		I-G	RAN,j y,k,b,s	Replace Add Negative to A: (A) − Y → Y & A
26	1	I-G	AQ,j y,k,b,s	Add to Q: (Q) + Y → Q
27	1	I-G	ANQ,j y,k,b,s	Add Negative to Q: (Q) − Y → Q
30		I-G	LSUM,j y,k,b,s	Load Sum: Y + (Q) → A
31		I-G	LDIF,j y,k,b,s	Load Difference: Y − (Q) → A
32	6	I-G	SSUM,j y,k,b,s	Store sum: (A) + (Q) → Y & A
33	6	I-G	SDIF,j y,k,b,s	Store Difference: (A) − (Q) → Y & A
34		I-G	RSUM,j y,k,b,s	Replace Sum: Y + (Q) → Y & A
35		I-G	RDIF,j y,k,b,s	Replace Difference: Y − (Q) → Y & A
36		I-G	RI,j y,k,b,s	Replace Increment: Y + 1 → Y & A
37		I-G	RD,j y,k,b,s	Replace Decrement: Y − 1 → Y & A
40	1	I-G	LLP,j y,k,b,s	Load Logical Product: L [Y(Q)] → A
41	6	I-G	ALP,j y,k,b,s	Add Logical Product: (A) + L [Y (Q)] → A
42	6	I-G	NLP,j y,k,b,s	Add Negative Logical Product: (A) − L[Y (Q)] → A
43		I-G	CM,j y,k,b,s	Compare Mask: (A) − L [Y(Q)] → A Sense j, (A) + L [Y (Q)] → A
44	1	I-G	RLP,j y,k,b,s	Replace Logical Product: L [Y(Q)] → Y & A
45	6	I-G	RALP,j y,k,b,s	Replace Add Logical Product: A + L [Y (Q)] → Y & A
46	6	I-G	RNLP,j y,k,b,s	Replace Add Negative Logical Product: (A) − L [Y (Q)] → Y & A
47	6	I-G	SLP,j y,k,b,s	Store Logical Product: L [(Q) (A)] → Y
50		I-G	OR,j y,k,b,s	Inclusive OR: Set $(A)_n$ for $Y_n = 1$
51		I-G	XOR,j y,k,b,s	Exclusive OR: Complement $(A)_n$ for $Y_n = 1$
52 k≠7		I-G	SC,j y,k,b,s	Selective Clear: Clear $(A)_n$ for $Y_n = 1$
53 k≠7	6	I-G	MS,j y,k,b,s	Masked Substitute: $Y_n \rightarrow A_n$ if $Q_n = 1$
54		I-G	ROR,j y,k,b,s	Replace OR: [Set $(A)_n$ for $Y_n = 1$] → Y & A
55		I-G	RXOR,j y,k,b,s	Replace Exclusive OR: [CPL $(A)_n$ for $Y_n = 1$] → Y & A

NOTES

1 See List of Special Designators
2 If $Y_{29,28} = 0$, Skip NI and (A) → Y; If $Y_{29,28} \neq 0$, Do NI
3 See List of Special d,e,c,m Designators
4 See List of Special Push, Pull Designators. nc = Non-Circular (Opt.) Otherwise Circular. If bit 20 = 1, Y_{6-4} must be 111
5 Instruction may be used on modified processors only

FUNCTION CODE	NOTES*	FORMAT	SYMBOLIC CODE SEQUENCE(S)	DESCRIPTION
56		I-G	RSC,j y,k,b,s	Replace Selective Clear: [Clear $(A)_n$ for $Y_n = 1$] → Y & A
57	6	I-G	RMS,j y,k,b,s	Replace Masked Substitute: [$(Y_n) \rightarrow A_n$ if $Q_n = 1$] → Y & A
60 j=0		I-G	RIL	Release Interrupt Lockout
60 j=1		I-G	JRIL y,k,b,s	Jump and Release Interrupt Lockout
60 j=2		I-G	JQP y,k,b,s	Jump if Q Positive
60 j=3		I-G	JQN y,k,b,s	Jump if Q Negative
60 j=4		I-G	JAZ y,k,b,s	Jump if A + Zero
60 j=5		I-G	JANZ y,k,b,s	Jump if A not + Zero
60 j=6		I-G	JAP y,k,b,s	Jump if A Positive
60 j=7		I-G	JAN y,k,b,s	Jump if A Negative
61 j=0		I-G	J y,k,b,s	Jump
61 j=1 - 7		I-G	JC,j y,k,b,s	Jump Conditional if Jump j is Selected
61 j=4 - 7		I-G	JSC,j y,k,b,s	Stop Conditional if Stop j Selected and Jump on Restart
62 j=0	7	I-OP	ICIN y,k,b,s	Load/Initiate Chain Input: = 4 Bit Channel Number
62 j=1	7	I-OP	ICOUT y,k,b,s	Load/Initiate Chain Output: = 4 Bit Channel Number
62 j=2	7	I-OP	IBIN y,k,b,s	Initiate Input or EF Buffer: = 4 Bit Channel Number
62 j=3	7	I-OP	IBOUT y,k,b,s	Initiate Output or EF Buffer: = 4 Bit Channel Number
63 j=0	7	I-OP	LCIN y,k,b,s	Load Input Chain Pointer: = 4 Bit Channel Number
63 j=1	7	I-OP	LCOUT y,k,b,s	Load Output Chain Pointer: = 4 Bit Channel Number
63 j=2	7	I-OP	LBIN y,k,b,s	Load Input BCW: = 4 Bit Channel Number
63 j=3	7	I-OP	LBOUT y,k,b,s	Load Output BCW: = 4 Bit Channel Number
64 j=2	6	I-G	RJQP y,k,b,s	Return Jump if Q Positive
64 j=3	6	I-G	RJQN y,k,b,s	Return Jump if Q Negative
64 j=4	6	I-G	RJAZ y,k,b,s	Return Jump if A + Zero
64 j=5	6	I-G	RJANZ y,k,b,s	Return Jump if A not + Zero
64 j=6	6	I-G	RJAP y,k,b,s	Return Jump if A Positive
64 j=7	6	I-G	RJAN y,k,b,s	Return Jump if A Negative
65 j=0		I-G	RJ y,k,b,s	Return Jump
65 j=1 - 7		I-G	RJC,j y,k,b,s	Return Jump Conditional if Jump j Selected
65 j=4 - 7		I-G	RJSC,j y,k,b,s	Stop if Stop j Selected and Return Jump on Restart
66 j=0		III	STOP	Unconditional Stop
66 j=1	7	III	TIO y	Terminate I/O on Channel n for $y_n = 1$
66 j=2	3	III	SIL,d,e,c,m y	Disable Interrupts on Channel n for $y_n = 1$
66 j=3	3	III	RIL,d,e,c,m y	Enable Interrupts on Channel n for $y_n = 1$
67 j=0	7	I-OP	SCIN y,k,b,s	Store Chain Input Pointer: = 4 Bit Channel Number
67 j=1	7	I-OP	SCOUT y,k,b,s	Store Chain Output Pointer: = 4 Bit Channel Number
67 j=2	7	I-OP	SBIN y,k,b,s	Store Input BCW: = 4 Bit Channel Number
67 j=3	7	I-OP	SBOUT y,k,b,s	Store Output BCW: = 4 Bit Channel Number
70 j=0	6	I-G	RP y,k,b,s	Repeat Next Instruction
70 j=1	6	I-G	RPI y,k,b,s	Repeat and Increment
70 j=2	6	I-G	RPD y,k,b,s	Repeat and Decrement
70 j=3	6	I-G	RPB y,k,b,s	Repeat with B Modification
70 j=4	6	I-G	RPX y,k,b,s	Repeat with Index
70 j=5	6	I-G	RPXI y,k,b,s	Repeat with Index and Increment
70 j=6	6	I-G	RPXD y,k,b,s	Repeat with Index and Decrement
70 j=7	6	I-G	RPBX y,k,b,s	Repeat with Index and B Modification
71		I-G	BSK j,y,k,b,s	(Bj) ≠ Y, Advance Bj; (Bj) = Y, Skip NI and Clear (Bj)
72 j=0		I-G	CPFI	Clear Program Fault Indicator. On Modified Processors, Also Clears Hardware Fault Indicator.
72 j≠0		I-G	JBNZ j,y,k,b,s	(Bj) ≠ 0, (Bj) − 1 → Bj and Jump to Y; (Bj) = 0 Read NI
73 j=0		I-G	JOVF y,k,b,s	Jump if Overflow Bit Set
73 j≠0		I-G	LBJ j,y,k,b,s	Load Bj and Jump
74 bit 20=0	4	IV	PULLT j,y,b,s	If Table Not Empty, Pull Top and Skip NI; else do NI
74 bit 20=1	4,5	IV	PULTB j,y,b,s	Pull Top Biased: If Table Not Empty, Pull Top and Skip NI Y Biased by Processor Number in Bits 6-4; else do NI
75 bit 20=0	4	IV	PULLB,nc j,y,b,s	If Table Not Empty, Pull Bottom and Skip NI; else do NI
75 bit 20=1	4,5	IV	PULBB,nc j,y,b,s	Pull Bottom Biased: If Table Not Empty, Pull Bottom and Skip NI Y Biased by Processor Number in Bits 6-4; else do NI
76 bit 20=0	4	IV	PUSHT,nc j,y,b,s	If Table Not Full, Push Top and Skip NI; else do NI
76 bit 20=1	4,5	IV	PSHTB,nc j,y,b,s	Push Top Biased: If Table Not Full, Push Top and Skip NI Y Biased by Processor Number in Bits 6-4; else do NI
7700	10	II-G	XM	Enable Executive Mode: Perform Executive Return
7701	6	II-G	TXM y,b,s	Terminate Executive Mode: 1 → Status Register$_6$ Jump to Y

NOTES

6 Instruction may be used on CPM's only
7 Instruction may be used on IOP's only
8 Instruction may be used on modified CPM only
9 Instruction may be used on unmodified processors only
10 Instruction may be used on modified IOP's or any CPM

FUNCTION CODE	NOTES*	FORMAT	SYMBOLIC CODE SEQUENCE(S)	DESCRIPTION
7702	5	V	PPL y	Push P to List: P → Address Specified by (1220) (1220) + 1 → 1220, Jump to y
7703 bit 15=0	5	II-G	PLP	Pull List to P: (1220) − 1 → 1220; Jump to (1220) f
7703 bit 15=1	5	II-G	PLPR	Pull List to P and Release Interrupt Lockout: (1220) − 1 → 1220; Jump to (1220) f
7704	5	II-G	ERAJ y,b,s	Enable Relative Addressing & Jump: 1 → Status Register$_6$; Jump to Y
7705		II-G	XR y,b,s	Execute Remote: Execute Instruction Located at Address Y
7707	8	II-G	DSF y,b,s	Double Scale Factor: Shift AQ Left Until $A_{29} \neq A_{28}$, but not More Than 59 Places. Shift Count → Y
7710	6	II-G	LBP y,b,s	Load Breakpoint Register: $(Y_{19-0}) \rightarrow$ Breakpoint Reg. if Switch in Program Position
7711	8	II-G	DL y,b,s	Double Length Load: (Y) → Q, (Y + 1) → A
7712	5	II-G	LAB y,b,s	Load A Biased: (Y + Processor Number) → A
7714	6	II-G	SBP y,b,s	Store Breakpoint Register: (Breakpoint Register) → Y_{19-0} $0 \rightarrow Y_{29-20}$
7715	8	II-G	DS y,b,s	Double Length Store: (Q) → Y and (A) → Y + 1
7716	5	II-G	SAB y,b,s	Store A Biased: (A) → Y + Processor Number
7720	8	II-G	FA y,b,s	Floating Add: F(Q, A) + F (Y, Y + 1) → QA
7721	8	II-G	FAN y,b,s	Floating Add Neg: F(Q, A) − F (Y, Y + 1) → QA
7722	8	II-G	FM y,b,s	Floating Multiply: F(Q, A) · F (Y, Y + 1) → QA
7723	8	II-G	FD y,b,s	Floating Divide: F(Q, A) ÷ F (Y, Y + 1) → QA
7724	8	II-G	DA y,b,s	Double Length Add: (A,Q) + (Y+1, Y) → AQ
7725	8	II-G	DAN y,b,s	Double Length Add Negative: (A,Q) − (Y + 1, Y) → AQ
7726		II-G	LMC y,b,s	Load and Enable Monitor Clock: Y → Monitor Clock
7727		II-G	TSF y,b,s	Test and Set Flag: If $Y_{29,28} = 0$, Skip NI & Set $Y_{29,28}$: If $Y_{29,28} \neq 0$, Do NI
7734	5	II-G	ER y,b,s	Establish Read: (Y) → A; If $(A)_{14-0} = 0$, 1 → Bit Position Corresponding to the Processor Number Within Y_{22-15} and Skip NI. If $(A)_{14-0} \neq 0$, Execute NI
7735	5	II-G	EW y,b,s	Establish Write: (Y) → A. If (A) = 0, 1 → Bit Position Corresponding to the Processor Number Within Y_{7-0} and Skip NI. If (A) ≠ 0, Execute NI.
7736	5	II-G	RR y,b,s	Relinquish Read; 0 → Bit Position Corresponding to the Processor Number Within Y_{22-15}
7737	5	II-G	RW y,b,s	Relinquish Write; 0 → Bit Position Corresponding to the Processor Number Within Y_{7-0}
7741 k=0	8	II- OP	DFR	Disable Floating Point Round: 0 → Status Register$_3$
7741 k=1	8	II- OP	EFR	Enable Floating Point Round: 1 → Status Register$_3$
7742 k=1		II-OP	LST y,b,s	Load Status Register: (Y) → Status Reg.
7743 k=1	5	II-OP	LML y,b,s	Load Memory Lockout Register: $(Y)_{15-0} \rightarrow$ MLOJ
7744 k=0	5	II-OP	SMLQ J	Store Memory Lockout Register in Q: (MLOJ) → Q_{15-0} (RARJ) → Q_{19-16} $0 \rightarrow Q_{29-20}$
7744 k=1	5	II-OP	SML y,b,s	Store Memory Lockout Register: (MLOJ → Y_{15-0} (RARJ → Y_{19-16} $0 \rightarrow Y_{29-20}$
7745 k=0		II-OP	SSTQ	Store Status Register: (Status Reg.) → Q
7745 k=1		II-OP	SST y,b,s	Store Status Register: (Status Reg.) → Y
7746 k=0	5	II-OP	DRPIR	Disable Relative Processor Interrupt Register: 0 → Status Register$_{11}$
7746 k=1	5	II-OP	ERPIR	Enable Relative Processor Interrupt Register: 1 → Status Register$_{11}$
7747 k=0	5	II-OP	LRPIR y	Load Relative Processor Interrupt Register: $Y_{2-0} \rightarrow$ RPJ
7747 k=1	5	II-OP	SRPIR J	Store Relative Processor Interrupt Register: (RPIJ → Q_{2-0} $0 \rightarrow Q_{29-3}$
7750	5	II-OP	DRAD	Disable Relative Address Designator: 0 → Status Register$_6$
7751	5	II-OP	LRAR y	Load Relative Address Register $Y_{3-0} \rightarrow$ RARJ
7760		II-OP	LSR j,y,k,b,s	Load Address Extension Register SRJ (J = 0,1,2): k = 0: $Y_{4-0} \rightarrow$ SRJ k = 1: $(Y)_{4-0} \rightarrow$ SRJ
7770		II-OP	SSR J,y,k,b,s	Store Address Extension Register SRJ (J = 0,1,2): k = 0: (SRJ → Q_{4-0} and Clear Q_{29-5} k = 1: (SRJ → Y_{4-0} and Clear Y_{14-5}

NOTES

* If no processor note (5-10) is referenced, instruction may be used on any processor

Y = The Operand Regardless of Source, i.e., y, (Y), Y or sy

Y = The Source or Destination of the Operand, i.e., y extended plus Bb

All non-existent function codes except $64_j = 0$ and $64_j = 1$ will cause control to be transferred to the program fault interrupt entrance address.

F(c,m) represents a floating point number with Characteristic in C & Mantissa in M

NORMAL k DESIGNATOR

k	READ		STORE		REPLACE			JUMP	
	MN.	Origin	MN.	Dest.	MN.	Origin	Dest.	MN.	Jump to Modulo 2^{18}
0	'blank'	sy + Bb	QR	Q	'not used'	–	–	'blank'	sy + Bb
1	L	$\underline{Y}_L$	L	Y_L	L	$\underline{Y}_L$	Y_L	L	$\underline{Y}_L$
2	U	$\underline{Y}_U$	U	Y_U	U	$\underline{Y}_U$	Y_U	U	$\underline{Y}_U$
3	W	$\underline{Y}$	W	Y	W	$\underline{Y}$	Y	W	$\underline{Y}$
4	RX	$X_{(sy)}$ + Bb	AS	A	'not used'	–	–	RX	Y_S + Bb
5	LX	XY_L	CPL	$\underline{Y}_L \rightarrow Y_L$	LX	XY_L	Y_L	LX	XY_L
6	UX	XY_U	CPU	$\underline{Y}_L \rightarrow Y_U$	UX	XY_U	Y_U	UX	XY_U
7	AR	A	CPW	$\underline{Y} \rightarrow Y$	'not used'	–	–	AR	(A)

$\underline{Y}$ = (Y_S + Bb)
Y_S = Selected SR (4-0) or P (17-13) concatenated with y (12-0)
sy = s (14-13) concatenated with y (12-0)
W = Whole word

L = Lower half
U = Upper half
X = Sign extension
CP = Complement
MN = Mnemonic

NORMAL b DESIGNATOR

b	MNEMONIC	DESCRIPTION
0	'blank'	No Mod
1	B1	B1
2	B2	B2
3	B3	B3
4	B4	B4
5	B5	B5
6	B6	B6
7	B7	B7

NORMAL j DESIGNATOR

j	MNEMONIC	DESCRIPTION
0	'blank'	No Skip
1	SK	Skip
2	QP	Skip if Q Positive.
3	QN	Skip if Q Negative
4	AZ	Skip if A + Zero
5	ANZ	Skip if A Not + Zero
6	AP	Skip if A Positive
7	AN	Skip if A Negative

SPECIAL $\hat{j}$ DESIGNATOR

$\hat{j}$	MN.	C f04	MN.	M f22	D f23	MN.	LLP f40	RLP f44	MN.	AQ f26	ANQ f27
0	'blank'	No Skip	'blank'	No Skip	No Skip	'blank'	No Skip		'blank'	No Skip	
1	SK:	Skip	SK:	Skip	Skip	SK:	Skip		SK:	Skip	
2	YLEQ:	$\underline{Y} = (Q)$	NOVF:	$Q_{29} = A_{29}$	No Over flow	EVEN:	Even Parity		AP:	A Positive	
3	YGTQ:	$\underline{Y} > (Q)$	OVF:	$Q_{29} \neq A_{29}$	Over flow	ODD:	Odd Parity		AN:	A Negative	
4	YIN:	$(A) < \underline{Y} \leq (Q)$	AZ:	A = ± Zero	A = ± Zero	AZ:	A + Zero		QZ:	Q + Zero	
5	YOUT:	$\underline{Y} > (Q)$ or $\underline{Y} \leq (A)$	ANZ:	A ≠ ± Zero	A ≠ ± Zero	ANZ:	A Not + Zero		QNZ:	Q Not + Zero	
6	YLEA:	$\underline{Y} \leq (A)$	6:	Skip	Skip	AP:	A Positive		QP:	Q Positive	
7	YGTA:	$\underline{Y} > (A)$	7:	No Skip	No Skip	AN:	A Negative		QN:	Q Negative	

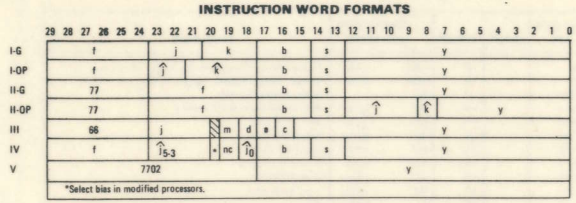
SPECIAL d,e,c,m, DESIGNATOR

DES	MNEMONIC	DESCRIPTION
d	ND	Normal Device Interrupts
e	EIS	External Interrupt & Status Word Storage
c	CI	Channel Interrupts (Class V)
m	M	Metronome, only applicable to modified processor

ADDRESS EXTENSION(s) DESIGNATOR

s	MNEMONIC	DESCRIPTION
0	S0	SR0
1	S1	SR1
2	S2	SR2
3	S3 or 'blank'	Bit 17-13 of P

INSTRUCTION WORD FORMATS



SPECIAL PUSH, PULL $\hat{j}$ DESIGNATORS

$\hat{j}_{5-3}$	$\hat{j}_0 = 0$	$\hat{j}_0 = 1$
0	RTC	S0 : SR0
1	B1	S1 : SR1
2	B2	S2 : SR2
3	B3	AR : A Reg.

$\hat{j}_{5-3}$	$\hat{j}_0 = 0$	$\hat{j}_0 = 1$
4	B4	QR : Q Reg.
5	B5	SR : Status Reg.
6	B6	UNDEFINED
7	B7	UNDEFINED

STATUS REGISTER BIT ASSIGNMENT

IOP STATUS REGISTER		CPM STATUS REGISTER	
BIT	DESCRIPTION	BIT	DESCRIPTION
2-0	Device Number	2-0	Device Number
3	Class 5 Interrupt Lockout	3	Floating Point Round Enable (modified only)
4	Class 4 Interrupt Lockout	4	Class 4 Interrupt Lockout
5	Class 3 Interrupt Lockout	5	Class 3 Interrupt Lockout
6	Relative Address Enable (modified only)	6	Relative Address Enable (modified only)
9	Scatter Interrupt Lockout (modified only)	7	B-register Select (unmodified only)
10	Arithmetic Overflow	8	Executive Mode Designator (unmodified only)
11	Interrupt Steering Enable (modified only)	9	Scatter Interrupt Lockout (modified only)
15-12	Channel Number	10	Arithmetic Overflow
18-16	Interrupt Type*	11	Interrupt Steering Enable (modified only)
22-19	Memory Module Number	18-16	Interrupt Type*
23	I/O Error	22-19	Memory Module Number
24	Operand Error	24	Operand Error
25	Instruction Error	25	Instruction Error
26	Memory Resume Error	26	Memory Resume Error
27	Address Parity Error	27	Address Parity Error
28	Data Parity Error	28	Data Parity Error
29	I/O Data Parity Error		

INTERRUPT TYPE CODES TABLE

BINARY	DESCRIPTION	PROCESSOR
000	Input Data Error (not parity)	IOP Only
001	Output Data Error	IOP Only
010	Write Lockout Violation (modified only)	Both
011	External Interrupt Error (not parity)	IOP Only
100	Input Chain Error	IOP Only
101	Output Chain Error	IOP Only
110	Read Lockout Violation (modified only)	Both
111	I/O Write Lockout Violation (modified only)	IOP Only

MEMORY LOCKOUT REGISTER (MLO)

BIT	DESCRIPTION
29-27	Interrupt Steering Register*
19-16	Relative Address Register*
15-8	Read Lockout
7-0	Write Lockout

NOTE: Lockout bits represent 2048 word blocks.

*Registers are for display and external setting.

I/O CONTROL MEMORY ADDRESS

BINARY	DESCRIPTION
0 0 C C C C	Input Chain Pointer
0 1 C C C C	Output Chain Pointer
1 0 C C C C	Input Buffer Control Word
1 1 C C C C	Output Buffer Control Word

NOTE: C C C C is channel number.

BREAKPOINT REGISTER (CPM ONLY)

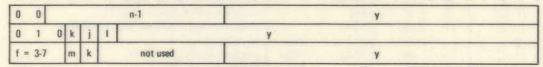
BIT	DESCRIPTION
19	Enable Operand Address Check
18	Enable Instruction Address Check
17-0	Address

SPERRY UNIVAC DEFENSE SYSTEMS

CHAIN INSTRUCTIONS

BINARY FUNCTION	SYMBOLIC CODE SEQUENCE(S)		DESCRIPTION
00	BCW	n,y	Buffer Control Word, n=number of words to be transferred
010 j=0, k=0	EFW	y,I	External Function: Whole Word, I=1 for Indirect
010 j=1, k=0	FEFW	y,I	Force External Function: Whole Word, I=1 for Indirect
010 j=1, k=1	EFH	y,I	External Function: Half Word, I=1 for Indirect
010 j=1, k=1	FEFH	y,I	Force External Function: Half Word, I=1 for Indirect
011	IOSTOP,m		I/O Stop, m=1 for Monitor Interrupt
100	IOCL	y	I/O Clear Flag: 0→ $y_{29,28}$
101	IOJ,m,k	y	I/O Jump, m=1 for Monitor Interrupt, k=1 insert channel number in y_{3-0}
110	IOSET	y	I/O Set Flag: 1→ $y_{29,28}$
111	IONOOP		I/O No Operation

CHAIN INSTRUCTION FORMATS



INTERRUPT ADDRESSES

INDIVIDUAL INTERRUPTS	ADDRESS (BINARY)
Power On Entrance w/Auto Start Selected (unmodified processor only)	1 00X XX0 001
Power Tolerance Entrance (unmodified processor only)	1 00X XX0 010
Executive Return Entrance (modified IOP or any CPM)	1 00X XX0 011
Breakpoint Entrance (CPM only)	1 00X XX0 100
I/O Write Lockout Entrance (unmodified IOP only)	1 00X XX0 110
Normal Device Entrance	1 00X XX1 001
Monitor Clock Entrance	1 00X XX1 010
Metronome Entrance (modified processor only)	1 00X XX1 011
Memory Write Lockout Entrance (unmodified processor only)	1 00X XX1 011
Memory Read Lockout Entrance (unmodified processor only)	1 00X XX1 111
Hardware Fault Entrance (unmodified processor only)	1 011 000 000
Program Fault Entrance	1 011 000 001
Scatter Interrupt Starting Address (modified processor only)	'1 011 000 010
Class V Interrupt Packet	
Status Buffer Control Word (BCW)	0 XXX CCC C00
Status BCW Refill	0 XXX CCC C10
Entrance Address	0 XXX CCC C11

* XXX implies 3-bit device number placed in address, thus completing relative address. CCC represents channel number.

PUSH, PULL CONTROL PARAMETER WORDS