AN/UYK-8(V) COMPUTER
REPERTOIRE OF INSTRUCTION

Octal Code	Symbolic Code	DESCRIPTION	Coding Sequence(s)	Format
00		Program Fault: Generate Class I Interrupt	f	
01	SRQ	Shift Right (Q) by Y	f, j y, k, b, s	I
02	SRA	Shift Right (A) by Y	f, j y, k, b, s	I
03	DSR	Double Shift Right (AQ) by Y	f, j y, k, b, s	I
*04j2	CQNL	Compare Q not less: (Q)≥Y	f y, k, b, s	I
*04j3	CQL	Compare Q less: (Q)<Y	f y, k, b, s	I
*04j4	CW	Compare Y within limits: (Q)>Y>(A)	f y, k, b, s	I
*04j5	CNW	Compare Y not within limits: Y>(Q) or Y<(A)	f y, k, b, s	I
*04j6	CNL	Compare A not less: (A)<Y	f y, k, b, s	I
*04j7	CL	Compare A less: (A)<Y	f y, k, b, s	I
05	SLQ	Shift Left (Q) by Y	f, j y, k, b, s	I
06	SLA	Shift Left (A) by Y	f, j y, k, b, s	I
07	DSL	Double Shift Left (AQ) by Y	f, j y, k, b, s	I
10	LQ	Load Q: Y→Q	f, j y, k, b, s	I
10	ZQ	Clear Q: 0→Q	f, j	I
11	LA	Load A: Y→A	f, j y, k, b, s	I
11	ZA	Clear A: 0→A	f, j	I
12	LB	Load Bⁱ: Y→Bⁱ	f j, y, k, b, s	I
12	ZB	Clear Bⁱ: 0→Bⁱ	f j	I
12j0	NOOP	No Operation: 0→B⁰	f	I
^13k0	FWM	1 Function Word with Monitor on Cⁱ	f j, y, b, s	I-I/O
^13k1	FWMF	1 Function Word with Force and Monitor on Cⁱ	f j, y, b, s	I-I/O
^13k2	FW	1 Function Word on Cⁱ	f j, y, b, s	I-I/O
^13k3	FWF	1 Function Word with Force on Cⁱ	f j, y, b, s	I-I/O
14	SQ	Store Q: (Q)→Y	f, j y, k, b, s	I
14k0	CPQ	Complement Q: (Q)'→Q	f, j	I
15	SA	Store A: (A)→Y	f, j y, k, b, s	I
15k4	CPA	Complement A: (A)'→A	f, j	I
16	SB	Store Bⁱ: (B)→Y	f j, y, k, b, s	I
16j0	SZ	Store Zero: (B)⁰→Y	f y, k, b, s	I
^17k0, 1	JFA	Jump Function Active on Cⁱ; Y →P	f j, y, k, b, s	I-I/O
^17k2	IWF	Input 1 word, Force on Cⁱ: (C)ⁱ→Y	f j, y, b, s	I-I/O
^17k3	SIW	Store Interrupt Word from Cⁱ: (000520+j)→Y	f j, y, b, s	I-I/O
20	AA	Add A: (A)+Y→A	f, j y, k, b, s	I
21	ANA	Add Negative A: (A)−Y→A	f, j y, k, b, s	I
22	M	Multiply: (Q) • Y→AQ	f, j y, k, b, s	I
*23	D	Divide: (AQ)÷Y→Q; remainder→A	f, j y, k, b, s	I
*23k7	RT	Square Root: $\sqrt{(Q)}$ →Q; remainder→A	f, j	
24	RA	Replace A+Y: (A)+Y→A & Y	f, j y, k, b, s	I
25	RAN	Replace A−Y: (A)−Y→A & Y	f, j y, k, b, s	I
*26	AQ	Add Q: (Q)+Y→Q	f, j y, k, b, s	I
*27	ANQ	Add Negative Q: (Q)−Y→Q	f, j y, k, b, s	I
30	LSUM	Load Y+Q: Y+(Q)→A	f, j y, k, b, s	I
31	LDIF	Load Y−Q: Y−(Q)→A	f, j y, k, b, s	I
32	SSUM	Store A+Q: (A)+(Q)→A & Y	f, j y, k, b, s	I
33	SDIF	Store A−Q: (A)−(Q)→A & Y	f, j y, k, b, s	I
34	RSUM	Replace Y+Q: Y+(Q)→A & Y	f, j y, k, b, s	I
35	RDIF	Replace Y−Q: Y−(Q)→A & Y	f, j y, k, b, s	I
36	RI	Replace Increment: Y+1→Y & A	f, j y, k, b, s	I
37	RD	Replace Decrement: Y−1→Y & A	f, j y, k, b, s	I
*40	LLP	Load Logical Product: L|Y(Q)|→A	f, j y, k, b, s	I
41	ALP	Add Logical Product: A+L|Y(Q)|→A	f, j y, k, b, s	I
42	NLP	Add Negative Logical Product: A−L|Y(Q)|→A	f, j y, k, b, s	I
43j2	CMQP	Compare Masked Q Positive	f y, k, b, s	I
43j3	CMQN	Compare Masked Q Negative	f y, k, b, s	I
43j4	CMZ	Compare Masked Zero: (A)−L|Y(Q)|→A, sense j,	f y, k, b, s	I
43j5	CMNZ	Compare Masked Not Zero: (A)+L|Y(Q)|→A; $A_f=A_i$	f y, k, b, s	I
43j6	CMP	Compare Masked Positive:	f y, k, b, s	I
43j7	CMN	Compare Masked Negative:	f y, k, b, s	I
*44	RLP	Replace Logical Product: L|Y(Q)|→A & Y	f, j y, k, b, s	I
45	RALP	Replace Add Logical Product: (A)+L|Y(Q)|→A & Y	f, j y, k, b, s	I
46	RNLP	Replace Add Negative Logical Product: (A)−L|Y(Q)|→A & Y	f, j y, k, b, s	I
47	SLP	Store Logical Product: L|(A)(Q)|→Y; $A_f=A_i$, $Q_f=Q_i$	f, j y, k, b, s	I
50	OR	Inclusive OR: Set $(A)_n$ for $Y_n=1$	f, j y, k, b, s	I
51	XOR	Exclusive OR: Complement $(A)_n$ for $Y_n=1$	f, j y, k, b, s	I
52	SC	Selective Clear: Clear $(A)_n$ for $Y_n=1$	f, j y, k, b, s	I
53	MS	Masked Selective Substitute: $Y_n \rightarrow A_n$ for $(Q)_n=1$	f, j y, k, b, s	I
54	ROR	Replace Inclusive OR: Set $(A)_n$ for $Y_n=1$ →A & Y	f, j y, k, b, s	I
55	RXOR	Replace Exclusive OR: Complement $(A)_n$ for $Y_n=1$ →A & Y	f, j y, k, b, s	I
56	RSC	Replace Selective Clear: Clear $(A)_n$ for $Y_n=1$ →A & Y	f, j y, k, b, s	I
57	RMS	Replace Masked Selective Sub: $(Y_n \rightarrow (A)_n$ for $(Q)_n=1$ →A & Y	f, j y, k, b, s	I
*60j0	RIL	Remove Interrupt L/O: Allow all interrupts not locked out by PEI	f	I
*60j1	JRIL	Jump Remove Interrupt L/O: Allow all interrupts not locked out by PEI and jump to Y	f y, k, b, s	I
*60j2	JQP	Jump Q Positive: Jump to Y if (Q) is positive	f y, k, b, s	I
*60j3	JQN	Jump Q Negative: Jump to Y if (Q) is negative	f y, k, b, s	I
*60j4	JZ	Jump A Zero: Jump to Y if (A) is positive zero	f y, k, b, s	I
*60j5	JNZ	Jump A Not Zero: Jump to Y if (A) is not zero	f y, k, b, s	I
*60j6	JP	Jump A Positive: Jump to Y if (A) is positive	f y, k, b, s	I
*60j7	JN	Jump A Negative: Jump to Y if (A) is negative	f y, k, b, s	I
*61j0	J	Jump: Jump to Y	f, j y, k, b, s	I
*61j1, 2, 3	JC	Jump to Y on conditional setting	f, j y, k, b, s	I
*61j4	JS	Jump to Y and stop	f y, k, b, s	I
*61j5, 6, 7	JSC	Jump to Y and stop on conditional setting	f, j y, k, b, s	I
^62	JIA	Jump Input Buffer Active on Cⁱ	f j, y, k, b, s	I-I/O
^63	JOA	Jump Output Buffer Active on Cⁱ	f j, y, k, b, s	I-I/O

* { Special j and/or k designation ($\hat{j}$, $\hat{k}$)

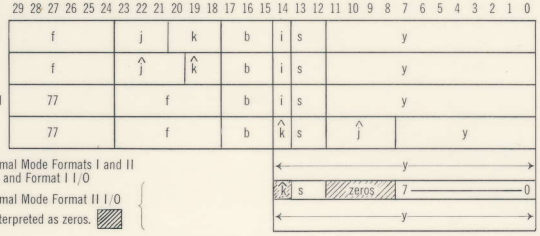
Y The operand regardless of source

Ŷ The source or destination of the operand as defined by k, k̂, C or f

AN/UYK-8(V) COMPUTER
REPERTOIRE OF INSTRUCTION

Octal Code	Symbolic Code	DESCRIPTION	Coding Sequence(s)	Format
*64j1	ARJ	Arithmetic Return Jump: NI address→Y, Y+I→P	f y, k, b, s	I
*64j2	RJQP	Return Jump Q Positive:	f y, k, b, s	I
*64j3	RJQN	Return Jump Q Negative:	f y, k, b, s	I
*64j4	RJZ	Return Jump A Zero: NI address→Y, Y+I→P	f y, k, b, s	I
*64j5	RJNZ	Return Jump Not Zero: if condition is satisfied	f y, k, b, s	I
*64j6	RJP	Return Jump A Positive:	f y, k, b, s	I
*64j7	RJN	Return Jump A Negative:	f y, k, b, s	I
*64j0	RJ	Return Jump: NI address→Y, Y+I→P	f, j y, k, b, s	I
*65j1, 2, 3	RJC	Return Jump on Jump Switch Setting; NI address→Y, Y+I→P	f, j y, k, b, s	I
*65j4	RJS	Return Jump and Stop; NI address→Y, Y+I→P	f y, k, b, s	I
*65j5, 6, 7	RJSC	Return Jump and Stop on Stop Switch Setting; NI address→Y, Y+I→P	f, j y, k, b, s	I
66k0	TIB	Terminate Input Buffer on Cⁱ	f j	I-I/O
66k1b0	AAI	Allow All Interrupts	f	I-I/O
66k1b1	PAI	Prevent All Class IV Interrupts	f	I-I/O
66k2b0	AAEI	Allow All External Interrupts	f	I-I/O
66k2b0	PAEI	Prevent All External Interrupts	f	I-I/O
66k3b0	AEI	Allow External Interrupts on Cⁱ	f j	I-I/O
66k3b0	PEI	Prevent External Interrupt on Cⁱ	f j	I-I/O
^67k0	TOB	Terminate Output Buffer on Cⁱ	f j	I-I/O
^67k1	TFB	Terminate Function Buffer on Cⁱ	f j	I-I/O
^67k2	TIO	Terminate I/O Buffers on all Channels	f	I-I/O
*70j0	RP	Repeat Next Instruction Y Times	f, j y, k, b, s	I
*70j1	RPI	Repeat, Increment	f y, k, b, s	I
*70j2	RPD	Repeat, Decrement	f y, k, b, s	I
*70j3	RPB	Repeat, Add B: Repeat next instruction	f y, k, b, s	I
*70j4	RPX	Repeat, Add Index: Y times and modify the	f y, k, b, s	I
*70j5	RPXI	Repeat, Add Index, Increment: operand address per *j	f y, k, b, s	I
*70j6	RPXD	Repeat, Add Index, Decrement	f y, k, b, s	I
*70j7	RPBX	Repeat, Add B, Index	f y, k, b, s	I
71	BSK	B Skip on Bⁱ: (B)ⁱ=Y, skip NI and clear (B)ⁱ; (B)ⁱ≠Y, advance Bⁱ and read NI	f j, y, k, b, s	I
72	JBNZ	Jump Bⁱ Not Zero: (B)ⁱ=0, read NI; (B)ⁱ≠0, (B)ⁱ−1→Bⁱ & jump to Y	f j, y, k, b, s	I
^73	IB	Input Buffer on Cⁱ: Y→000100+j or 001100+j	f j, y, k, b, s	I-I/O
^74	OB	Output Buffer on Cⁱ: Y→000120+j or 001120+j	f j, y, k, b, s	I-I/O
^74k2	FB	Function Buffer on Cⁱ: Y→000140+j or 001140+j	f j, y, b, s	I-I/O
^75	IBM	Input Buffer, Monitor, on Cⁱ: Y→000100+j or 001100+j	f j, y, k, b, s	I-I/O
^76	OBM	Output Buffer, Monitor, on Cⁱ: Y→000120+j or 001120+j	f j, y, k, b, s	I-I/O
^76k2	FBM	Function Buffer, Monitor, on Cⁱ: Y→000140+j or 001140+j	f j, y, b, s	I-I/O
77 00	XM	Enter Executive Mode: 0→Status Reg. Bit 24, Set Class III L/O, Jump to 000010	f	
77 01	TXM	Terminate Executive Mode: 1→Status Reg. Bit 24, (Y)→P	f y, b, s	II
77 02	LBJ	Load B and Jump: (P)+1→B³, (Y)→P	f y, b, s	II
77 03	JOF	Jump on Arithmetic Overflow: Clear overflow Des., if Set and Jump to Y, otherwise do NI	f y, b, s	II
77 05	XR	Execute Remote Instruction: Read NI from address Y	f y, b, s	II
77 07	DSF	Double Precision Scale Factor: Left shift (AQ) until A29≠A28; Shift count→Y	f y, b, s	II
77 10	LBP	Load Breakpoint Register: Y_{15-0}→breakpoint Reg.	f y, b, s	II
77 11	DL	Double Precision Load: (Y)→Q, (Y+1)→A	f y, b, s	II
77 12	LDR	Load Display Register: (Y)→Display Reg.	f y, b, s	II
77 14	SBP	Store Breakpoint Register: (Breakpoint Reg.)→Y	f y, b, s	II
77 15	DS	Double Precision Store: (Q)→Y, (A)→Y+1	f y, b, s	II
77 16	SDR	Store Display Register: (Display Reg.)→Y	f y, b, s	II
77 17	CNT	Count ones in (Y) Count→A	f y, b, s	II
77 20	FA	Floating Point Add: FP(Y, Y+1) + FP(AQ)→AQ normalized	f y, b, s	II
77 21	FAN	Floating Point Add Negative: FP(AQ) − FP(Y, Y+1)→AQ Normalized	f y, b, s	II
77 22	FM	Floating Point Multiply: FP(AQ)×FP(Y, Y+1)→AQ normalized	f y, b, s	II
77 23	FD	Floating Point Divide: FP(AQ)÷FP(Y, Y+1)→AQ normalized quotient	f y, b, s	II
77 24	DA	Double Precision Add: (AQ) + (Y+1, Y)→AQ	f y, b, s	II
77 25	DAN	Double Precision Add Negative: (AQ) − (Y+1, Y)→AQ	f y, b, s	II
77 27	TSF	Test and Set Flag: (Q) Neg., L|Y(Q)|→A&Y, Skip NI; (Q) Pos. &(A)=0, (Q)∨Y→Y, Skip NI; (Q) Pos. &(A)≠0, Y→Y, Read NI	f y, b, s	II
77 33	LII	Load I/O Interrupt Assignment Register: (Y)→IAR	f y, b, s	II
77 36	LMC	Load and Enable Monitor Clock: $(Y_{17-0}$→RTC Monitor Reg.; Enable Decrement	f y, b, s	II
77 37	SII	Store I/O Interrupt Assignment Register: (IAR)→Y	f y, b, s	II
77 41k1	FR	Floating Point Round Enable: Set Status Reg. bit 19	f	II-I/O
77 41k0	TFR	Terminate Floating Point Round: Clear Status Reg. bit 19	f	II-I/O
77 42k1	LST	Load Status Register: (Y)→Status Reg.	f y, b, s	II-I/O
^77 43k1	LML	Load Memory Lockout Reg.: $(Y_{15-0}$→MLO	f j, y, b, s	II-I/O
^77 44	SML	Store Memory L/O Reg.: k=0, (MLO)→Q; k=1, (MLO)ⁱ→Y_{15-0}	f j, y, k, b, s	II-I/O
^77 45	SST	Store Status Reg.: k=0, (Status Reg.)→Q, k=1, (Status Reg.)→Y	f y, k, b, s	II-I/O
^77 60	LSR	Load Relative Address Reg.; k=0, Y_{15-0}→RAR⁰; k=1, Y_{15-0}→RAR¹	f j, y, k, b, s	II-I/O
^77 61	LIX	Load Input Ext. Reg. C⁰: k=0, Y_{2-0}→Input Ext. Reg. C⁰; k=1, Y_{2-0}→Input Ext. Reg. Cⁱ	f j, y, k, b, s	II-I/O
^77 62	LOX	Load Output Ext. Reg. C⁰: k=0, Y_{2-0}→Output Ext. Reg. C⁰; k=1, Y_{2-0}→Output Ext. Reg. Cⁱ	f j, y, k, b, s	II-I/O
^77 63	LFX	Load Function Ext. Reg. C⁰: k=0, Y_{2-0}→EF Ext. Reg. C⁰; k=1, Y_{2-0}→EF Ext. Reg. Cⁱ	f j, y, k, b, s	II-I/O
^77 64	ICD	Enable Input Continuous Data Mode on Cⁱ	f j	II-I/O
^77 65	OCD	Enable Output Continuous Data Mode on Cⁱ	f j	II-I/O
^77 66	TICD	Terminate Input CDM on Cⁱ	f j	II-I/O
^77 67	TOCD	Terminate Output CDM on Cⁱ	f j	II-I/O
^77 70	SSR	Store Relative Address Reg.: k=0, (RAR)⁰→Q_{5-0}; k=1, (RAR)¹→Y_{5-0}	f j, y, k, b, s	II-I/O
^77 71	SIX	Store Input Extension Reg. C⁰: (Input Ext. Reg.)→Y_{2-0}	f j, y, k, b, s	II-I/O
^77 72	SOX	Store Output Extension Reg. C⁰: (Output Ext. Reg.)→Y_{2-0}	f j, y, k, b, s	II-I/O
^77 73	SFX	Store Function Ext. Reg. C⁰: (Function Ext. Reg.)→Y_{2-0}	f j, y, k, b, s	II-I/O
^77 74	TXA	Terminate Expanded Address Mode: Clear Status Reg. bit 21	f	II-I/O
^77 75	XA	Expanded Address Mode Enable: Set Status Reg. bit 21	f	II-I/O
^77 76	LIOC	Load I/O Controller Designator: Select controller k+1, k→status Reg. bit 20	f k	II-I/O
77 77		Program Fault: Generate Class I Interrupt	f	II-I/O

AN/UYK-8
INSTRUCTION WORD FORMAT



The elements of the function word format are interpreted as follows:

- f — a 6-bit Function Code Designator
- i — a 1-bit Indirect Addressing Designator
- j — a 3-bit Branch Condition Designator
- ĵ — a 4-bit Input/Output Channel Designator, Special Register Designator, or Memory Lockout Register Designator
- k or k̂ — a 1-, 2-, or 3-bit Operand Interpretation Designator
- b — a 3-bit Index Register Designator
- s — a 2-bit Address Extension Designator
- y — a 15-, 13-, or 8-bit Operand or Address Designator

LEGEND

- M—Memory word (30 bits)
- M_L—Lower half memory word
- M_U—Upper half memory word
- X—Sign bit extended
- Cpl—Complement
- A—A-register
- Q—Q-register
- U_L—U-register, lower half

NORMAL k-DESIGNATORS

k	READ Origin	STORE Dest.	REPLACE Origin	REPLACE Dest.
0	U_L	Q	Not Used	
1	M_L	M_L	M_L	M_L
2	M_U	M_U	M_U	M_U
3	M	M	M	M
4	XU_L	A	Not Used	
5	XM_L	Cpl M_L	XM_L	M_L
6	XM_U	Cpl M_U	XM_U	M_U
7	A	Cpl M	Not Used	

NORMAL i-DESIGNATORS

j	(Not applicable on * or ^) Skip Code
0	No Skip
1	Skip
2	Q Pos
3	Q Neg
4	A Zero
5	A Not Zero
6	A Pos
7	A Neg

JUMP & RETURN JUMP ĵ & *j-DESIGNATORS

j	f60, f64	f61, f65
0	No Jump	Uncond. Jump
1	Uncond. Jump	Key 1
2	Q Pos	Key 2
3	Q Neg	Key 3
4	A Zero	Stop
5	A Not Zero	Stop 5
6	A Pos	Stop 6
7	A Neg	Stop 7
ĵ	62ĵ	63ĵ
$0\text{-}17_8$	C^a Active in	C^a Active out

#60 j0, 1 Clears interrupt & bootstrap modes.

SPECIAL k̂ DESIGNATOR FORMAT II

k̂	Read Origin	Store Destination Justified Right
0	U_L	Q
1	M	M

SPECIAL *i-DESIGNATORS

	SKIP CONDITIONS					ADDRESS MODIFICATION OF REPEATED INSTRUCTION	
j	f04	f23k7̄	f26, f27	f40, f44	f23k7	f70	
0	No Skip	No Skip	No Skip	No Skip	No Skip	Y of NE=Y	
1	Skip	Skip	Skip	Skip	Skip	Y of NE=Y+1	
2	Y≤(Q)	No Overflow	A Pos	Even Parity	Not Used	Y of NE=Y−1	
3	Y≥(Q)	Overflow	A Neg	Odd Parity	Not Used	Y of NE=Y+B^b	
4	(Q)≥Y>(A)	A Zero	Q Zero	A Zero	No Rem	Y of NE=Y|+B^6|	√
5	(Q)<Y or Y≤(A)	A Not Zero	Q Not Zero	A Not Zero	Rem	Y of NE=Y+1|+B^6|	√
6	Y≤(A)	Skip	Q Pos	A Pos	Not Used	Y of NE=Y−1|+B^6|	√
7	Y≥(A)	No Skip	Q Neg	A Neg	Not Used	Y of NE=Y+B^b|+B^6|	√

√ If NI is RPL class, B^6 increments Y address for the store portion of the replace.
NE—Next execution

UNIVAC
FEDERAL SYSTEMS DIVISION
St. Paul, Minnesota

AN/UYK-8
MEMORY ADDRESS ASSIGNMENT

	Assignment	Central Processors	For Input/Output Controller #1	For Input/Output Controller #2
DRO Main Memory	Program Fault Entrance	000		
	Reserved	001		
	Power Restart Interrupt Entrance	002		
	Power Tolerance Interrupt Entrance	003		
	Breakpoint Interrupt Entrance	004		
	Processor 1 Normal NDRO Exit	005		
	Processor 2 Normal NDRO Exit	006		
	NDRO Hardware Analysis Status	007		
	Executive Entrance	010		
	Executive Error Interrupt Entrance	011		
	Write Lockout Interrupt Entrance	012		
	Read Lockout Interrupt Entrance	013		
	Characteristic Overflow Interrupt Entrance	014		
	Characteristic Underflow Interrupt Entrance	015		
	Floating Point Divide Error Interrupt Entrance	016		
	Monitor Clock Interrupt Entrance		017	1017
	External Interrupt Entrance		020-037	1020-1037
	Input Monitor Interrupt Entrance		040-057	1040-1057
	Output Monitor Interrupt Entrance		060-077	1060-1077
I.C. Control Memory In I/O Controller	Input Buffer Control Register		100-117	1100-1117
	Output Buffer Control Register		120-137	1120-1137
	External Function Buffer Control Register		140-157	1140-1157
	Real Time Clock		160	1160
	Unassigned		161-167	1161-1167
	Monitor Clock		170	1170
	NDRO Hardware Analysis Storage		171-177	
	Reserved			1171-1177
DRO Main Memory	ESI Input Terminate or CDM Reload		200-217	1200-1217
	ESI Output Terminate or CDM Reload		220-237	1220-1237
	ESI External Function Terminate		240-257	1240-1257
	Unassigned	260-477		
	External Function Monitor Interrupt Entrance		500-517	1500-1517
	External Interrupt Word Store		520-537	1520-1537
	NDRO Hardware Analysis Bank 1 Error Exit—Processor 1	540		
	NDRO Hardware Analysis Bank 1 Error Exit—Processor 2	541		
	Reserved for NDRO	542-577		
	Intercomputer Timeout Interrupt Entrance		600-617	1600-1617
	Unassigned	620-1016		
	Unassigned	1260-1477		
	Unassigned	1540-1577		
	Unassigned	1620-1777		
NDRO Memory	Bootstrap Program 0 Entrance	2000		
	Bootstrap Program 1 Entrance	2001		
	Bootstrap Program 2 Entrance	2002		
	Hardware Fault Interrupt Entrance	2003		
	Bootstrap and Hardware Fault Programs	2004-2777		
DRO Main Memory	Unassigned	3000-77775		
	NDRO Hardware Analysis Bank 0 Error Exit—Processor 1	77776		
	NDRO Hardware Analysis Bank 0 Error Exit—Processor 2	77777		
	Expanded Memory (option) Unassigned Storage	100000-777777		