UNIVAC MTC
REPERTOIRE OF INSTRUCTIONS

Code (Octal) f	INSTRUCTION	DESCRIPTION	Time μsec.
01	Right SHift•Q	Shift (Q) Right by Y	1.8
02	Right SHift•A	Shift (A) Right by Y	1.8
03	Right SHift•AQ	Shift (AQ) Right by Y	1.8
*04	COMpare•A, •Q, •AQ	Compare Y with A, Q or A & Q; A_i=A_f	1.8
05	Left SHift•Q	Shift (Q) Left by Y	1.8
06	Left SHift•A	Shift (A) Left by Y	1.8
07	Left SHift•AQ	Shift (AQ) Left by Y	1.8
10	ENTer•Q	Y→Q	1.8
10	CLear•Q	0→Q	1.8
11	ENTer•A	Y→A	1.8
11	CLear•A	0→A	1.8
12	ENTer•B^n	Y→B^j	3.6**
12	CLear•B^n	0→B^j	3.6**
12	NO-OPeration	0→B^n (do nothing operation)	3.6**
^13k0	EXternal-COMmand•C^n•W(Y)•MONITOR	(Y)→C^j	3.6
^13k1	EXcom-COMmand•C^n•W(Y)•MONFORCE	(Y)→C^j (use on CP-642A equipment)	3.6***
^13k2	EXternal-COMmand•C^n•W(Y)	(Y)→C^j	3.6
^13k3	EXternal-COMmand•C^n•W(Y)•FORCE	(Y)→C^j (use on CP-642A equipment)	3.6***
14	SToRe•Q	(Q)→Y	1.8
14k0	ComPlement•Q	Q'→Q	1.8
15	SToRe•A	(A)→Y	1.8
16	SToRe•B^n	$(B)^j$→Y	1.8
^17k0	JumP•Y•C^n•COMACTIVE	Jump to Y if external buffer active	3.6
^17k1	JumP•L(Y)•C^n•COMACTIVE	Jump to (Y)L if external function active	3.6
17k2	SToRe•C^n•W(Y)•FORCE	Force C^j→(Y)–(abnormal test mode)	3.6
^17k3	SToRe•C^n•W(Y)	(00520+j)→(Y)	3.6
20	ADD•A	(A)+Y→A	1.8
21	SUBtract•A	(A)–Y→A	1.8
22	MULtiply	(Q)Y→AQ	7.2*
*23	DIVide	(AQ) Y→Q; R→A_f	12.6*
*23k7	SQuare RooT	$\sqrt{Q}$→Q; remainder→A	7.2*
24	RePLace•A+Y	(A)+(Y)→Y&A	3.6
25	RePLace•A–Y	(A)–(Y)→Y&A	3.6
*26	ADD•Q	(Q)+Y→Q	1.8
*27	SUBtract•Q	(Q)–Y→Q	1.8
30	ENTer•Y+Q	Y+Q→A	1.8
31	ENTer•Y–Q	Y–Q→A	1.8
32	SToRe•A+Q	(A)+(Q)→Y&A	3.6
33	SToRe•A–Q	(A)–(Q)→Y&A	3.6
34	RePLace•Y+Q	(Y)+(Q)→Y&A	3.6
35	RePLace•Y–Q	(Y)–(Q)→Y&A	3.6
36	RePLace•Y+1	(Y)+1→Y&A	3.6
37	RePLace•Y–1	(Y)–1→Y&A	3.6
*40	ENTer•LP	L[Y(Q)]→A	1.8
41	ADD•LP	(A)+L[Y(Q)]→A	1.8
42	SUBtract•LP	(A)–L[Y(Q)]→A	1.8
43	COMpare•MASK	(A)–L[Y(Q)sense (j); A+L[Y(Q)]; $(A)_i$=$(A)_f$	1.8
*44	RePLace•LP	L(Y)(Q)→Y&A	3.6
*45	RePLace•A+LP	(A)+L(Y)(Q)→Y&A	3.6
46	RePLace•A–LP	(A)–L(Y)(Q)→Y&A	3.6
47	SToRe•LP	L(A)(Q)→Y; $(A)_i$=$(A)_f$	1.8
50	SELective•SET	Set $(A)_n$ for Y_n=1	1.8
51	SELective•ComPlement	Complement $(A)_n$ for Y_n=1	1.8
51k4	ComPlement•A	If Y is 77777, A'→A	1.8
52	SELective•CLear	Clear $(A)_n$ for Y_n=1	1.8
53	SELective•SUbstitute	Y_n→$(A)_n$ for $(Q)_n$=1	1.8
54	Replace SE l ective•SET	[Set $(A)_n$ for $(Y)_n$=1]→Y&A	3.6
55	Replace SE l ective•CP	[Complement $(A)_n$ for $(Y)_n$=1]→Y&A	3.6
56	Replace SE l ective•CL	[Clear $(A)_n$ for $(Y)_n$=1]→Y&A	3.6
57	Replace SE l ective•SU	[$(Y)_n$→$(A)_n$ for $(Q)_n$=1]→Y&A	3.6
*60	JumP (arithmetic)	Jump to Y if j-condition is satisfied	3.6**
60j0	Remove Interrupt Lockout	Enable all interrupts not locked out by SIL-EX	1.8**
60j1	Remove Interrupt Lockout JumP•Y	Enable interrupts and jump to Y	3.6**
*61	JumP (manual)	Jump to Y if j-condition is satisfied	3.6**
^62	JumP on•C^n•ACTIVE INput buffer	Jump to Y if C^j input buffer active	3.6*
^63	JumP on•C^n•ACTIVE OUTput buffer	Jump to Y if C^j output buffer active	3.6*

* [Special j and k designators
Y—The operand; Y or (Y)

**Execution time is constant
***Program held until transfer is completed.

UNIVAC MTC
REPERTOIRE OF INSTRUCTIONS

Code (Octal) f	INSTRUCTION	DESCRIPTION	Time μsec.
*64	Return JumP (arithmetic)	Jump to Y+1 and (P)+1→Y_L if j-condition	5.4
*65	Return JumP (manual)	is satisfied (see JP and RJP j-designators)	5.4**
^66	TERMinate•C^n•INPUT	Terminate input buffer on C^j	1.8
^66k1	Remove Interrupt Lockout•ALL	Enable all interrupts not locked out by SIL-EX	1.8
^66k2	Remove Interrupt Lockout-EXternal•ALL	Enable external interrupts; all channels	1.8
^66k3	Remove Interrupt Lockout-EXternal•C^n	Enable external interrupts on C^j	1.8
^66k1b1	Set Interrupt Lockout•ALL	Lockout all interrupts on all channels	1.8
^66k2b1	Set Interrupt Lockout-EXternal•ALL	Lockout external interrupts; all channels	1.8
^66k3b1	Set Interrupt Lockout-EXternal•C^n	Lockout external interrupt on C^j	1.8
^67	TERMinate•C^n•OUTPUT	Terminate output buffer on C^j	1.8
^67k1	TERMinate•C^n•COMmand	Terminate external function buffer on C^j	1.8
^67k2	TERMinate•ALL	Terminate ALL buffers	3.6**
*70	RePeaT	Execute NI Y times	
71	BSKip•B^n	$(B)^j=Y$, skip NI and clear $(B)^j$; $(B)^j\neq Y$, advance B^j and read NI	3.6**
72	BJumP•B^n	$(B)^j=0$, read NI; $(B)^j\neq 0$, $(B)^j-1\rightarrow B^j$ & jump to Y	3.6**
^73	INput•C^n (without monitor mode)	Buffer in on C^j; Y→00100+j	3.6**
^74	OUTput•C^n (without monitor mode)	Buffer out on C^j; Y→00120+j	3.6**
^74k2	EXternal-COMmand-MultiWord•C^n•W(Y)	Buffer commands out on C^j; (Y)→00140+j	3.6**
^75	INput•C^n (with•MONITOR mode)	Buffer in on C^j with monitor; Y→00100+j	3.6**
^76	OUTput•C^n (with MONITOR mode)	Buffer out on C^j with monitor; Y→00120+j	3.6**
^76k2	EX-COM-MultiWord•C^n•W(Y)•MONITOR	Buffer commands out on C^j with monitor; (Y)→00140+j	3.6**
7700	Enable Executive Mode	0→Status Reg 2^9 bit, Lockout Class III Interrupts and Enter Exec Mode Loc. 10	3.6
7701	EXit Executive Mode	1→Status Reg 2^9 bit, Remove Interrupt Lockout and Y→P	3.6
7702	Load B and JumP	(P)+1→B7 and jump to Y Ignore Indirect Addressing	3.6
7703	Test OverFlow Designator	Clear overflow designator, if set, and jump to Y; otherwise do NI	3.6
7705	EXecute Remote Instruction	Read NI from address Y, Ignore Indirect Addressing	1.8
7707	NORMalize•AQ	Shift AQ left until $A_{29}\neq A_{28}$; Shift count→Y	3.6
7710	Enter BreakPoint Register	Y_{19-0}→Breakpoint Register if switch in PROG. position	1.8
7711	Double length ENTer	(Y)→Q& (Y+1)→A	3.6
7713	Enter Indirect Address Designator	Y_{6-0}→Status Register bits 2^6-2^0	1.8
7714	Store BreakPoint Register	(Breakpoint Reg)→Y_{19-0}; Clear Y upper	1.8
7715	Double length SToRe	(Q)→Y and (A)→Y+1	3.6
7720	Floating point ADD	FP (Y, Y+1)+FP (AQ)→AQ normalized	7.2**
7721	Floating point SUBtract	FP (AQ)−FP (Y, Y+1)→AQ normalized	7.2**
7722	Floating point MULtiply	FP(AQ)×FP(Y, Y+1)→AQ normalized	10.8**
7723	Floating point DIVide	FP(AQ)÷FP(Y, Y+1)→AQ normalized quotient	16.2**
7724	Double length ADD	(Q)+(Y)→Q; (A)+(Y+1)→A	3.6
7725	Double length SUBtract	(Q)−(Y)→Q; (A)−(Y+1)→A	3.6
7726	Set and Enable Monitor Clock	Y_{17-0}→RT Monitor Register, enable decrementing	1.8**
7727	Test and Set Flag	Test Y_{29-28} & L(Q)(Y) Skip or execute NI and Set Y_n	3.6
7735	InterProcessor Interrupt	Initiate the interrupt to other processor	1.8**
7740	Enter I O Interrupt Assignment Register	Y→I O Interrupt assignment Status Reg.	1.8
^7741	Enable Disable Floating Point Round	If k=0 disable if k=1 enable FP round	1.8
7742k1	Enter STatus Register	Y→STATUS	1.8
7743k1	Enter Memory Lockout Register	Y→MLO_j	1.8
^7744	Store Memory Lockout Register	If k=0, MLO_j→Q_{15-0}; if k=1, MLO_j→Y_{15-0}	1.8
^7745	Store STatus Register	If k=0 STATUS→Q; if k=1 STATUS→Y	1.8
7746	Store I O Interrupt Assignment Register	I O Int. Assign. and Status Reg→Y_{28-0} and 0→Y_{29}	1.8
7760	ENTer SR^n; (n=0, 1 or 2)	Y_{4-0}→SR	1.8
^7761	ENTer SR•C^n•Y•INPUT	Y_{2-0}→Input SR-Channel j	1.8
^7762	ENTer SR•C^n•Y•OUTPUT	Y_{2-0}→Output SR-Channel j	1.8
^7763	ENTer SR•C^n•Y•EF	Y_{2-0}→External Function SR-Channel j	1.8
7764	Enable CDM•C^n•INPUT	Enable Input Channel j CDM	1.8**
^7765	Enable CDM•C^n•OUTPUT	Enable Output Channel j CDM	1.8**
^7766	Disable CDM•C^n•INPUT	Disable Input Channel j CDM	1.8**
^7767	Disable CDM•C^n•OUTPUT	Disable Output Channel j CDM	1.8**
7770	SToRe SR^n; (n=0, 1 or 2)	(SR^j)→Y_{4-0}	1.8
^7771	SToRe SR•C^n•Y•INPUT	(SR^j)→Y_{2-0}; for Channel j Input	1.8
^7772	SToRe SR•C^n•Y•OUTPUT	(SR^j)→Y_{2-0}; for Channel j Output	1.8
^7773	SToRe SR•C^n•Y•EF	(SR^j)→Y_{2-0}; for Channel j External function	1.8
7774	Disable EXPanded memory code	Disable 18-bit addressing mode	1.8**
7775	Enable EXPanded memory mode	Enable 18-bit addressing mode	1.8**
^7776	Select I/O Controller^n (n=1 or 2)	Select Controller k+1; k→$STATUS_{14}$	1.8**

*, ^ Special j and k designators
Y—The operand; Y or (Y)

**Execution time is constant

MEMORY ADDRESS ASSIGNMENT

		NDRO Core & Chip	Input-Output Controller	
			#I	#II
Main Memory	Program Fault Entrance	00000		
	Power Restart Interrupt Entrance	001		
	Power Tolerance Interrupt Entrance	002		
	Interprocessor Interrupt Entrance	003		
	Breakpoint Interrupt Entrance	004		
	Reserved	005		
	Reserved	006		
	Reserved	007		
	Executive Entrance	010		
	Executive Error Interrupt Entrance	011		
	Write Lockout Interrupt Entrance	012		
	Read Lockout Interrupt Entrance	013		
	Characteristic Overflow Interrupt Entrance	014		
	Characteristic Underflow Interrupt Entrance	015		
	Floating Point Divide Error Interrupt Entrance	016		
	Monitor Clock Interrupt	017		
	External Interrupt Entrance		020-037	1020-1037
	Input Monitor Interrupt Entrance		040-057	1040-1057
	Output Monitor Interrupt Entrance		060-077	1060-1077
Control Memory	Input Buffer Control Register		100-117	1100-1117
	Output Buffer Control Register		120-137	1120-1137
	External Function Buffer Control Register		140-157	1140-1157
Main Memory	Real Time Clock		160	1160
Chip Memory	Index Registers	161-167		
Main Memory	Unassigned	170-177		
	ESI Input Terminate or CDM Reload		200-217	1200-1217
	ESI Output Terminate or CDM Reload		220-237	1220-1237
	ESI External Function Terminate		240-257	1240-1257
	Unassigned	260-277		
NDRO	Hardware Fault Interrupt Entrance	300		
	Hardware Fault Analysis Routine	301-377		
Main Memory	Unassigned	400-477		
	External Function Monitor Interrupt Entrance	500-517		
	External Interrupt Code Store	520-537		
	Unassigned	540-577		
	Intercontroller Timeout Interrupt Entrance	600-617		
	Unassigned	620-677		
NDRO Memory	Load Program I (Entrance—700)	700-737		
	Load Program II (Entrance—740)	740-777		
Main Memory	Unassigned	1000-1017		
		1161-1177		
		1260-1477		
	External Function Monitor Interrupt Entrance	1500-1517		
	External Interrupt Word Storage	1520-1537		
	Unassigned	1540-1577		
	Intercomputer Time-Out Entrance	1600-1617		
	Unassigned	1620-77777		
	Expanded Memory Option—Unassigned	100000-777777		

MEMORY ADDRESS ASSIGNMENT

		NDRO Core & Chip	Input-Output Controller	
			#I	#II
Main Memory	Program Fault Entrance	00000		
	Power Restart Interrupt Entrance	001		
	Power Tolerance Interrupt Entrance	002		
	Interprocessor Interrupt Entrance	003		
	Breakpoint Interrupt Entrance	004		
	Reserved	005		
	Reserved	006		
	Reserved	007		
	Executive Entrance	010		
	Executive Error Interrupt Entrance	011		
	Write Lockout Interrupt Entrance	012		
	Read Lockout Interrupt Entrance	013		
	Characteristic Overflow Interrupt Entrance	014		
	Characteristic Underflow Interrupt Entrance	015		
	Floating Point Divide Error Interrupt Entrance	016		
	Monitor Clock Interrupt	017		
	External Interrupt Entrance		020-037	1020-1037
	Input Monitor Interrupt Entrance		040-057	1040-1057
	Output Monitor Interrupt Entrance		060-077	1060-1077
Control Memory	Input Buffer Control Register		100-117	1100-1117
	Output Buffer Control Register		120-137	1120-1137
	External Function Buffer Control Register		140-157	1140-1157
Main Memory	Real Time Clock		160	1160
Chip Memory	Index Registers	161-167		
Main Memory	Unassigned	170-177		
	ESI Input Terminate or CDM Reload		200-217	1200-1217
	ESI Output Terminate or CDM Reload		220-237	1220-1237
	ESI External Function Terminate		240-257	1240-1257
	Unassigned	260-277		
NDRO	Hardware Fault Interrupt Entrance	300		
	Hardware Fault Analysis Routine	301-377		
Main Memory	Unassigned	400-477		
	External Function Monitor Interrupt Entrance	500-517		
	External Interrupt Code Store	520-537		
	Unassigned	540-577		
	Intercontroller Timeout Interrupt Entrance	600-617		
	Unassigned	620-677		
NDRO Memory	Load Program I (Entrance—700)	700-737		
	Load Program II (Entrance—740)	740-777		
Main Memory	Unassigned	1000-1017		
		1161-1177		
		1260-1477		
	External Function Monitor Interrupt Entrance	1500-1517		
	External Interrupt Word Storage	1520-1537		
	Unassigned	1540-1577		
	Intercomputer Time-Out Entrance	1600-1617		
	Unassigned	1620-77777		
	Expanded Memory Option—Unassigned	100000-777777		