OCTAL CODE f	a	m	DESCRIPTION	SYMBOLIC CODES RR	RI	RK	RX	Exec Time Memory Cycles RR	RI	RK	RX	NOTE REF.
00			Byte Load	—	—	—	BL	—	—	—	3	
01			Load	LR	LI	LK	L	1	2	2	3	
02		0	Make Positive	PR	—	—	—	1	—	—	—	
		1	Make Negative	NR	—	—	—	1	—	—	—	
		2	Round R_a	RR	—	—	—	1	—	—	—	
		4	Two's Complement Single	TCR	—	—	—	1	—	—	—	
		5	Two's Complement Double	TCDR	—	—	—	1	—	—	—	
		6	One's Complement Single	OCR	—	—	—	1	—	—	—	
		10	Increase R_a by 1	IROR	—	—	—	1	—	—	—	
		11	Decrease R_a by 1	DROR	—	—	—	1	—	—	—	
		12	Increase R_a by2	IRTR	—	—	—	1	—	—	—	
		13	Decrease R_a by 2	DRTR	—	—	—	1	—	—	—	
02			Load Double	—	LDI	—	LD	—	3	—	4	
03		0	Executive Return	ER	—	—	—	1	—	—	—	
		1	Store Status Register 1	SSOR	—	—	—	1	—	—	—	
		2	*Store Status Register 2	SSTR	—	—	—	1	—	—	—	
		3	*Store RTC	SCR	—	—	—	1	—	—	—	
		4	Load P	LPR	—	—	—	1	—	—	—	
		5	Load Status Register 1	LSOR	—	—	—	1	—	—	—	1
		6	*Load Status Register 2	LSTR	—	—	—	1	—	—	—	
		7	*Load RTC	LCR	—	—	—	1	—	—	—	
		10	*Enable RTC	ECR	—	—	—	1	—	—	—	
		11	*Disable RTC	DCR	—	—	—	1	—	—	—	
		12	*Load and Enable INT. Clock	LEM	—	—	—	1	—	—	—	
03			Load Multiple	—	—	—	LM	—	—	—	2	2
04		0	*Square Root	SQR	—	—	—	1	—	—	—	3
		1	*Reverse Register	RVR	—	—	—	1	—	—	—	4
		2	*Count Ones	CNT	—	—	—	1	—	—	—	4
		3	*Scale Factor Shift	SFR	—	—	—	1	—	—	—	5
04			Byte Load and Index by 1	—	—	—	BLX	—	—	—	3	
05			*Set Bit	SBR	—	—	—	1	—	—	—	
05			Load and Index by 1	—	LXI	—	LX	—	2	—	3	
06			*Clear bit (Zero Bit)	ZBR	—	—	—	1	—	—	—	
06			Load Double and Index by 2	—	LDXI	—	LDX	—	3	—	4	
07			*Test Bit	CBR	—	—	—	1	—	—	—	
07			Load PSW	—	LPI	—	LP	—	3	—	4	
10			Logical Right Single Shift	LRSR	—	LRS	—	1	—	2	—	6
10			Byte Store	—	—	—	BS	—	—	—	3	
11			Algebraic Right Single Shift	ARSR	—	ARS	—	1	—	2	—	6
11			Store	—	SI	—	S	—	2	—	3	
12			Logical Right Double Shift	LRDR	—	LRD	—	1	—	2	—	6
12			Store Double	—	SDI	—	SD	—	3	—	4	
13			Algebraic Right Double Shift	ARDR	—	ARD	—	1	—	2	—	6
13			Store Multiple	—	—	—	SM	—	—	—	2	
14			Algebraic Left Single Shift	ALSR	—	ALS	—	1	—	2	—	6
14			Byte Store and Index by 1	—	—	—	BSX	—	—	—	3	
15			Circular Left Single Shift	CLSR	—	CLS	—	1	—	2	—	6
15			Store and Index by 1	—	SXI	—	SX	—	2	—	3	
16			Algebraic Left Double Shift	ALDR	—	ALD	—	1	—	2	—	6
16			Store Double and Index by 2	—	SDXI	—	SDX	—	3	—	4	
17			Circular Left Double Shift	CLDR	—	CLD	—	1	—	2	—	6
17			Store Zeros	—	SZI	—	SZ	—	2	—	3	
20			Subtract	SUR	SUI	SUK	SU	1	2	2	3	
21			Subtract Double	SUDR	SUDI	—	SUD	1	3	—	4	1
22			Add	AR	AI	AK	A	1	2	2	3	
23			Add Double	ADR	ADI	—	AD	1	3	—	4	1
24			Compare	CR	CI	CK	C	1	2	2	3	
25			Compare Double	CDR	CDI	—	CD	1	3	—	4	1
26			Multiply	MR	MI	MK	M	1	2	2	3	7
27			Divide	DR	DI	DK	D	1	2	2	3	7
30			AND	ANDR	ANDI	ANDK	AND	1	2	2	3	
31			OR	ORR	ORI	ORK	OR	1	2	2	3	
32			Exclusive OR	XORR	XORI	XORK	XOR	1	2	2	3	
33			Masked Substitute	MSR	MSI	MSK	MS	1	2	2	3	
34			Compare Masked	CMR	CMI	CMK	CM	1	2	2	3	
35			I/O Command	IOCR	—	—	—	1	—	—	—	
35			Biased Fetch	—	BFI	—	BF	—	2	—	3	
35			Execute Remote	—	—	REX	—	—	—	2	—	8

OCTAL CODE			DESCRIPTION	SYMBOLIC CODES				Exec Time Memory Cycles				NOTE REF.
f	a	m		RR	RI	RK	RX	RR	RI	RK	RX	
36			Processor-Peripheral Command	–	–	–	PTC	–	–	–	3	
37			*CORDIC	–	–	–	–	–	–	–	–	
40	0		Jump CC Zero/Equal	JER	–	JE	JE	1	–	2	3	
	1		Jump CC Not Zero/Not Equal	JNER	–	JNE	JNE	1	–	2	3	
	2		Jump CC Pos/Greater Than or Equal	JGER	–	JGE	JGE	1	–	2	3	
	3		Jump CC Neg/Less Than	JLSR	–	JLS	JLS	1	–	2	3	
	4		Jump on Overflow	JOR	–	JO	JO	1	–	2	3	
	5		Jump on Carry	JCR	–	JC	JC	1	–	2	3	9
	6		Jump Power Out	JPTR	–	JPT	JPT	1	–	2	3	
	7		Jump Bootstrap 2	JBR	–	JB	JB	1	–	2	3	
	10		Jump	JR	–	J	J	1	–	2	3	
	11		Jump Stop	JSR	–	JS	JS	1	–	2	3	
	12		Jump Stop Key 1	JKSR	–	JKS	JKS	1	–	2	3	
	13		Jump Stop Key 2	JKSR	–	JKS	JKS	1	–	2	3	
	16		Jump P-P Channel Active	JCAR	–	JCA	JCA	1	–	2	3	
40			Local Jump	–	LJ	–	–	–	#1	–	–	10
41			Index Jump	XJR	–	XJ	XJ	1	–	2	3	9
42			Jump and Link Register	JLRR	–	JLR	JLR	1	–	2	3	9
43			Local Jump and Link Memory	–	LJLM	–	–	–	#2	–	–	11
43			Jump and Link Memory	–	–	JLM	JLM	–	–	2	3	12
44			Jump Register Zero	JZR	–	JZ	JZ	1	–	2	3	9
44			Local Jump Equal	–	LJE	–	–	–	#1	–	–	10
45			Jump Register Not Zero	JNZR	–	JNZ	JNZ	1	–	2	3	9
45			Local Jump Not Equal	–	LJNE	–	–	–	#1	–	–	10
46			Jump Register Positive	JPR	–	JP	JP	1	–	2	3	9
46			Local Jump Greater Than or Equal	–	LJGE	–	–	–	#1	–	–	10
47			Jump Register Negative	JNR	–	JN	JN	1	–	2	3	9
47			Local Jump Less Than	–	LJLS	–	–	–	#1	–	–	10
70	0		Master Clear	ACR	–	–	–	1	–	–	–	
	2		Enable All Chains	ACR	–	–	–	1	–	–	–	
	3		Disable All Chains	ACR	–	–	–	1	–	–	–	
	4		Enable All External Interrupts	ACR	–	–	–	1	–	–	–	
	5		Disable All External Interrupts	ACR	–	–	–	1	–	–	–	
	6		Enable All External Monitors	ACR	–	–	–	1	–	–	–	
	7		Disable All External Monitors	ACR	–	–	–	1	–	–	–	
	10		Master Clear	CCR	–	–	–	1	–	–	–	
	12		Enable Chan. a Chain	CCR	–	–	–	1	–	–	–	
	13		Disable Chan. a Chain	CCR	–	–	–	1	–	–	–	
	14		Enable Chan. a Ext. Int.	CCR	–	–	–	1	–	–	–	
	15		Disable Chan. a Ext. Int.	CCR	–	–	–	1	–	–	–	
	16		Enable Chan. a Ext. Int. Monitor	CCR	–	–	–	1	–	–	–	
	17		Disable Chan. a Ext. Int. Monitor	CCR	–	–	–	1	–	–	–	
70			Initiate IO Transfer	–	–	–	IO	–	–	–	4	
71			Initiate Chain (Comm)	–	–	ICK	–	–	–	2	–	
71			Load CM (Chain)	–	–	LCMK	LCM	–	–	2	3	
71			Write (Load) CM (Comm)	–	–	–	WCM	–	–	–	3	
72			Read (Store) CM (Comm)	–	–	–	RCM	–	–	–	3	
72			Store CM (Chain)	–	–	–	SCM	–	–	–	3	
73	0		Halt	HCR	–	–	–	1	–	–	–	
73	1		Interrupt	IPR	–	–	–	1	–	–	–	
73	1		Set Flag	–	–	–	SF	–	–	–	3	
73	0		Clear Flag	–	–	–	ZF	–	–	–	3	

Footnotes:

* Optional instruction

\# RI, Type 1 Format

1 Add 750 nanoseconds

2 Plus the number of registers

3 Add 5.55 microseconds

4 Add 3.15 microseconds

5 Plus 750 nanoseconds and 150 nanoseconds times number of places shifted.

6 Plus 600 nanoseconds and 150 nanoseconds times number of places shifted.

7 RR and RK Format add 3.0 microseconds; RI and RX Format add 2.5 microseconds

8 Plus remote instruction time

9 RR Format add 450 nanoseconds; RK and RX Formats add 300 nanoseconds – if no jump, execution time is 1 cycle plus 300 nanoseconds.

10 Add 300 nanoseconds

11 Add 150 nanoseconds.

12 Add 150 nanoseconds – if no jump, execution time is 1 cycle plus 300 nanoseconds.

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