SPERRY UNIVAC
DEFENSE SYSTEMS
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S-3A
SPERRY UNIVAC® 1832
TECHNICAL SUMMARY

UDS 77648

CHRISTY

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1	II	51, 22 27, 28 29	J74	x, FF	TACCO MPD	28
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5	I	48, 12 21, 22 23, 29	J74	A, V B, W C, X D, Z E, a F, b G, c	Unit 1 - SRS Unit 2 - NDRC 1 Unit 3 - INSI Unit 4 - ~~RIU~~ Spare Unit 5 - T. Incos Unit 6 - RAAWS Unit 7 - ~~ECM~~ PDP-1	20 17 18 19 1 7 21
6	I	~~48~~, 49 13, 22 29, 52	J74	H, d J, e L, f M, g N, h P, i R, j	Unit 1 - AACS Unit 2 - NDRC 2 Unit 3 - DGVS Unit 4 - AHRS Unit 5 - CPINCOS Unit 6 - MAD Unit 7 - SESCOS	22 23 13 14 3 8 15
7	I	50, 14 22, 23 29, 52	J74	S, m T, n p, BB r, CC s, DD t, u v, w	Unit 1 - SLU Unit 2 - Spare Unit 3 - Spare Unit 4 - Spare Unit 5 - Spare Unit 6 - Spare Unit 7 - Spare	9
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9	I	~~54~~, 16 22, 23 30, 52	J75		~~Growth~~ Discrete Unit 7 HACLCS (6) (1883)	
10	PAR	48, 49 50, ~~53~~ 47 30	J71 J72		Parallel Ch. 47B (bits 24-31)	
11	I	24, 30 47			Test	

RESTART Switch J75

A. I/O CHANNEL ASSIGNMENTS

CHAN	TYPE	CARD LOC.	IOI-1 JACK	PIN	SUBSYSTEM	ID
0	III	52, 21 25, 26 27, 28	J78	z, AA	~~TACCO ADP~~ LH S 2 A & C 1	24
1	II	51, 22 27, 28 29	J74	z, AA	~~SENSO MPD~~ CP MPD	26
2	II	51, 22 27, 28 29	J74	z, AA	SPARE	27
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5	I	48, 12 21, 22 23, 29	J78	A, V B, W C, X D, Z E, a F, b G, c	Unit 1 - S. Incos Unit 2 - ~~ATR~~ Unit 3 - Spare Unit 4 - FLIR Unit 5 - ARMCOS Unit 6 - Spare Unit 7 - ~~Spare~~ ESM	2 12 5 6
6	I	49 13, 22 29, 52	J78	H, d J, e L, f M, g N, h P, i R, j	Unit 1 - DMTU Unit 2 - Spare Unit 3 - Spare Unit 4 - Spare Unit 5 - Spare Unit 6 - Spare Unit 7 - Spare	16
7	I	50, 14 22, 23 19, 52	J78	S, m T, n p, BB r, CC s, DD t, u v, w	Unit 1 - ~~ADP~~ PDP-2 Unit 2 - SRX Unit 3 - P. Incos Unit 4 - ~~Spare~~ RIU Unit 5 - Spare Unit 6 - Spare Unit 7 - Spare	10 11 4
8	~~I~~ IV	~~53~~, 15 22, 23 30, 52	J75		~~Spare~~ HARPOON (5) Serial Unit 3 - output Unit 5 - Input (1880)	
9	I	~~54~~, 16 22, 23 30, 52	J75	7 bit switch	~~Growth~~ Discrete Unit 7 HACLCS (5) (1885)	
10	PAR	45, 49 50, ~~53~~ 30 47	J76 J77		Parallel Ch. SAU 47B (bits 24-31)	
11	I	24, 30 47			Test	

Code	Mnemonic	NAME	DESCRIPTION	F	CA	R	UF	Time‡ μs
01 0	OR	Inclusive OR (Selective Set A)	(Y) ⊕ (A_a)→A_a	II	Y	Y	2	1.3
01 1	SC	Selective Clear A	(A_a) ⊙ (Y)'→A_a	II	Y	Y	2	1.3
01 2	MS	Selective Substitute	(Y)$_n$→(A_{a+1})$_n$ for all (A_a)$_{n=1}$; (A_a)$_{i=}$(A_a)$_f$	II	Y	Y	2	1.3
01 3	XOR	Exclusive OR (Sel. Comp. A)	(Y) ⊕ (A_a)→A_a; (A_{a+1})'→(A_a)$_n$ for (Y)$_{n=1}$	II	Y	Y	2	1.3
01 4	ALP	Add Logical Product	(A_{a+1}) + (Y) ⊙ (A_a)→A_{a+1}; (A_a)$_{i=}$(A_a)$_f$	II	Y	Y	2	1.3
01 5	LLP	Load Logical Product	(Y) ⊙ (A_a)→A_a	II	Y	Y	2	1.3
01 6	NLP	Subtract Logical Product	(A_{a+1})–(Y) ⊙ (A_a)→A_{a+1}; (A_a)$_{i=}$(A_a)$_f$	II	Y	Y	2	1.3
01 7	LLPN	Load Logical Product Next	(Y) ⊙ (A_a)→A_{a+1}; (A_a)$_{i=}$(A_a)$_f$	II	Y	Y	2	1.3
02 0	CNT	Count Ones	No. of Bits Set in (Y)→A_a	II	Y	Y	2	11.8
02 2	XR	Execute Remote	(Y)→U	II	N	N	8	1.6
02 3	XRL	Execute Remote Lower	(Y)$_L$→U	II	N	N	8	1.6
02 4	SLP	Store Logical Product	(A_{a+1}) ⊙ (A_a)→Y; (A_a)$_{i=}$(A_a)$_f$; (A_{a+1})$_{i=}$(A_{a+1})$_f$	II	Y	Y	2	2.3†
02 5	SSUM	Store Sum	(A_a)+(A_{a+1})→A_{a+1} & Y; (A_a)$_{i=}$(A_a)$_f$	II	Y	Y	2	2.3†
02 6	SDIF	Store Difference	(A_{a+1})–(A_a)→A_{a+1} & Y; (A_a)$_{i=}$(A_a)$_f$	II	Y	Y	2	2.3†
02 7	DS	Double Store A	A_{a+1}, A_a→Y+1, Y	II	N	N	2	3.4
03 0	ROR	Replace Inclusive OR	(Y) ⊕ (A_a)→A_a & Y	II	Y	Y	2	2.6
03 1	RSC	Replace Selective Clear	(A_a) ⊙ (Y)'→A_a & Y	II	Y	Y	2	2.6
03 2	RMS	Replace Selective Substitute	(Y)$_n$→(A_{a+1})$_n$ & Y for all (A_a)$_{n=1}$; (A_a)$_{i=}$(A_a)$_f$	II	Y	Y	2	2.6
03 3	RXOR	Replace Exclusive OR	(Y) ⊕ (A_a)→A_a & Y; (A_a)$_n$'→A_a & Y for Y$_{n=1}$	II	N	Y	2	2.6
03 4	RALP	Replace A+Logical Product	(A_{a+1})+(Y) ⊙ (A_a)→A_{a+1} & Y; (A_a)$_{i=}$(A_a)$_f$	II	Y	Y	2	2.6
03 5	RLP	Replace Logical Product	(Y) ⊙ (A_a)→Y & A_{a+1}; (A_a)$_{i=}$(A_a)$_f$	II	Y	Y	2	2.6
03 6	RNLP	Replace A–Logical Product	(A_{a+1})–(Y) ⊙ (A_a)→A_{a+1} & Y; (A_a)$_{i=}$(A_a)$_f$	II	Y	Y	2	2.6
03 7	TSF	Test and Set Flag	If (Y)$_{31}$=0, CD Set EQUAL. 1→Y$_{31}$ If (Y)$_{31}$=1, CD Set UNEQUAL.	II	N	Y	8	2.05
05 0	DL	Double Load A	(Y+1, Y)→A_{a+1}, A_a	II	N	N	2	2.5
05 1	DA	Double Add A	(A_{a+1}, A_a)+(Y+1, Y)→A_{a+1}, A_a	II	N	N	2	3.1
05 2	DAN	Double Subtract A	(A_{a+1}, A_a)–(Y+1, Y)→A_{a+1}, A_a	II	N	N	2	3.1
05 3	DC	Double Compare	Compare (A_{a+1}, A_a) to (Y+1, Y), Set CD	II	N	N	2	2.5
05 4	LBMP	Load Base and Memory Protection	(Y)$_{17-0}$→S_a; (Y-1)$_{20-0}$→SPR_a; Y→SIR_a Privileged if; ASR bit 8=0, $s \neq 7$, $a=7$	II	N	N	2	7.7
06 0	FA	Floating-point Add	Shift (A_{a+1}) or (Y+1) Right such that (A_a)=(Y) (A_{a+1})+(Y+1)→A_{a+1}; Normalize	II	N	N	2	7.9
06 1	FAN	Floating-point Subtract	Shift (A_{a+1}) or (Y+1) Right such that (A_a)=(Y) (A_{a+1})–(Y+1)→A_{a+1}; Normalize	II	N	N	2	7.9
06 2	FM	Floating-point Multiply	(A_a)+(Y)→(A_a) (A_{a+1}) • (Y+1)→A_{a+1}; Normalize	II	N	N	2	14.5
06 3	FD	Floating-point Divide	(A_a)–(Y)→(A_a) (A_{a+1})÷(Y+1)→A_{a+1}; Normalize	II	N	N	2	14.5
06 4	FAR	Floating-point Add with Round	Same as FA with (A_{a+1}) rounded	II	N	N	2	9.1
06 5	FANR	Floating-point Subtract w/Rd.	Same as FAN with (A_{a+1}) rounded	II	N	N	2	9.1
06 6	FMR	Floating-point Multiply w/Rd.	Same as FM with (A_{a+1}) rounded	II	N	N	2	14.5
06 7	FDR	Floating-point Divide w/Rd.	Same as FD with (A_{a+1}) rounded	II	N	N	2	14.5
07 0 a=0	XS	Enter Executive State	sy+(Bb)→CMR 156; Enter class IV (Executive)	II	N	N	11	5.0†
07 0* a=1	IPI	Interprocessor Interrupt	Send Class II interrupt to processors n (0-1) Specified by (sy+Bb)$_{n=1}$	II	N	N	11	5.0†
07 1**	AEI	Allow Enable Interrupt	Allow Monitor interrupts from IOCa on Channels n; where (sy+Bb)$_{n=1}$	II	N	N	6	3.8†
07 2**	PEI	Prevent Enable Interrupt	Prevent Monitor interrupts from IOCa on channels n; where (sy+Bb)$_{n=1}$	II	N	N	6	3.8†
07 3**	LIM	Load IOC Monitor Clock	sy+(Bb)→IOCa MON CLK	II	N	N	6	3.8†
07 4**	IO	Initiate I/O	Initiate IOCa at address Y	II	N	N	2	3.8†
07 5*	IR	Interrupt Return	Return to State Specified by DSW	II	N	N	9	3.75†
07 6	RP	Repeat	Repeat N.I.B; Times; sy + Bb(of N.I.)→Bb each cycle	II	N	N	6	1.3
10	LA	Load A	Y→A_a	I	Y	Y	1	1.3
11	LXB	Load A and Index B	Y→A_a; (Bb)+1→Bb	I	Y	N	1	2.2†
12	LDIF	Load Difference	Y–(A_a)→A_{a+1}; (A_a)$_{i=}$(A_a)$_f$	I	Y	Y	1	1.3
13	ANA	Subtract A	(A_a)–Y→A_a	I	Y	Y	1	1.3

Code	Mnemonic	NAME	DESCRIPTION	F	CA	R	UF	Time‡ μs
14	AA	Add A	(A_a)+Y→A_a	I	Y	Y	1	1.3
15	LSUM	Load Sum	(A_a)+Y→A_{a+1}; (A_a)$_{i=}$(A_a)$_f$	I	Y	Y	1	1.3
16	LNA	Load Negative	Y'→A_a	I	Y	Y	1	1.3
17	LM	Load Magnitude	|Y|→A_a	I	Y	Y	1	1.3
20	LB	Load B	Y→B_a	I	Y	Y	1	2.35
21	AB	Add B	(B_a)+Y→B_a; B_a zero extended	I	Y	Y	1	2.65
22	ANB	Subtract B	(B_a)–Y→B_a; B_a zero extended	I	Y	Y	1	2.65
23	SB	Store B	(B_a)→Y	I	Y	Y	1	1.7
24	SA	Store A	(A_a)→Y	I	Y	Y	1	1.7
25	SXB	Store A and Index B	(A_a)→Y; (Bb)+1→Bb	I	Y	N	1	2.2†
26	SNA	Store Negative	(A_a)'→Y	I	Y	Y	1	2.3†
27	SM	Store Magnitude	|(A_a)|→Y	I	Y	Y	1	2.3†
32	BZ	Clear Bit	0→Y_{ak}	I	N	Y	3	2.6
33	BS	Set Bit	1→Y_{ak}	I	N	Y	3	2.6
34	RA	Replace Add	(A_a+(Y)→A_{a+1} & Y; (A_a)$_{i=}$(A_a)$_f$	I	Y	Y	1	2.6
35	RI	Replace Increment	(Y)+1→A_a & Y	I	Y	Y	1	2.6
36	RAN	Replace Subtract	(Y)–(A_a)→A_{a+1} & Y; (A_a)$_{i=}$(A_a)$_f$	I	Y	Y	1	2.6
37	RD	Replace Decrement	(Y)–1→A_a & Y	I	Y	Y	1	2.6
40	M	Multiply A	(A_a) • Y→A_{a+1}, A_a	I	Y	Y	1	12.1
41	D	Divide A	(A_{a+1}, A_a)÷Y→A_a; Remainder→A_{a+1}	I	Y	Y	1	12.1
42	BC	Compare Bit to Zero	If (Y)$_{ak}$=1, CD Set EQUAL If (Y)$_{ak}$=1, CD Set UNEQUAL	I	N	Y	3	1.6
43	CXI	Compare Index Increment	If (B_a) ≥ Y, CD Set OUTSIDE, 0→B_a If (B_a) < Y, CD Set WITHIN, (B_a)+1→B_a	I	Y	Y	1	2.95
44	C	Compare	Compare (A_a) to Y, Set the CD	I	Y	Y	1	1.3
45	CL	Compare Limits	If (A_{a+1}) > Y ≥ (A_a), Set CD WITHIN	I	Y	Y	1	1.6
46	CM	Compare Masked	Compare (A_{a+1}) to (A_a) ⊙ Y, Set the CD	I	Y	Y	1	1.3
47	CG	Compare Gated	Compare |Y–(A_a)| to (A_{a+1}), Set the CD	I	Y	Y	1	2.2
50 0	JEP	Jump on Even Parity	If (A_{a+1}) ⊙ (A_a) is Even Parity, jump to Y	III	N	N	1	3.55†
50 1	JOP	Jump on Odd Parity	If (A_{a+1}) ⊙ (A_a) is Odd Parity, jump to Y	III	N	N	1	3.55†
50 2	DJZ	Jump Double Precision Zero	If (A_{a+1}, A_a)=0, jump to Y	III	N	N	1	3.25†
50 3	DJNZ	Jump Double Precision Not Zero	If (A_{a+1}, A_a)≠0, jump to Y	III	N	N	1	3.25†
51 0	JP	Jump A Positive	If (A_a) ≥ 0, jump to Y	III	N	N	1	3.25†
51 1	JN	Jump A Negative	If (A_a) < 0, jump to Y	III	N	N	1	3.25†
51 2	JZ	Jump A Zero	If (A_a)=0, jump to Y	III	N	N	1	3.25†
51 3	JNZ	Jump A Not Zero	If (A_a) ≠ 0, jump to Y	III	N	N	1	3.25†
52 0	LBJ	Load B and Jump	P +1→B_a, jump to Y	III	N	N	1	2.5†
52 1	JBNZ	Index Jump B	If (B_a) ≠ 0, then (B_a)–1→B_a, jump to Y	III	N	N	1	3.55†
52 2	JS	Jump sy+B	Jump to sy+(Bb)	III	N	N	13	2.5†
52 3	JL	Unconditional Jump Lower	Jump to the Lower of Y	III	N	N	12	2.5†
53 0 a=0	JNF	Jump on No Overflow	If OD is not Set, jump to Y; Clear OD	III	N	N	12	2.5†
53 0 a=1	JOF	Jump on Overflow	If OD is Set, jump to Y; Clear OD	III	N	N	12	2.5†
53 1 a=0	JNE	Jump on Not Equal	If CD ≠, jump to Y	III	N	N	12	2.5†
53 1 a=1	JE	Jump on Equal	If CD =, jump to Y	III	N	N	12	2.5†
53 1 a=2	JG	Jump on Greater Than	If CD >, jump to Y	III	N	N	12	2.5†
53 1 a=3	JGE	Jump on Greater Than or Equal	If CD ≥, jump to Y	III	N	N	12	2.5†
53 1 a=4	JLT	Jump on Less Than	If CD <, jump to Y	III	N	N	12	2.5†
53 1 a=5	JLE	Jump on Less Than or Equal	If CD ≤, jump to Y	III	N	N	12	2.5†
53 1 a=6	JNW	Jump Outside Limits	If CD Outside Limits, jump to Y	III	N	N	12	2.5†
53 1 a=7	JW	Jump Within Limits	If CD Within Limits, jump to Y	III	N	N	12	2.5†
53 2	RJ	Return Jump	P+1→Y, jump to Y+1	III	N	N	12	3.3†
53 2	RJC	Return Jump a=1, 2, 3	If switch a is Set, P+1→Y, jump to Y+1	III	N	N	1	3.3†
53 2*	RJSC	Return Jump a=4, 5, 6, 7	If switch a is Set, Stop; P+1→Y; jump to Y+1	III	N	N	1	3.3†
53 3	J	Manual Jump	Jump to Y	III	N	N	12	2.5†
53 3	JC	Manual Jump a=1, 2, 3	If switch a is Set, jump to Y	III	N	N	1	2.5†
53 3*	JSC	Manual Jump a=4, 5, 6, 7	If switch a is Set, Stop; Jump to Y	III	N	N	1	2.55†
54	LCT	Load CMR Task	(Y)→CMR_{ak}	I	N	Y	3	2.35
55*	LCI	Load CMR Interrupt	(Y)→CMR_{ak+100}	I	N	Y	3	2.35

Code	Mnemonic	NAME	DESCRIPTION	F	CA	R	UF	Time‡ μs
56√	SCT	Store CMR Task	$(CMR_{AK})\rightarrow Y$	I	N	Y	3	2.6†
57*	SCI	Store CMR Interrupt	$(CMR_{AK+100})\rightarrow Y$	I	Y	Y	3	2.6†
60√i=0	HSCT	Store CMR in A	$(CMR_{AK})\rightarrow A_b$	IV A	N	N	4	2.35†
60*i=1	HSCI	Store CMR in A	$(CMR_{AK+100})\rightarrow A_b$	IV A	N	N	4	2.35†
61√i=0	HLCT	Load CMR with A	$(A_b)\rightarrow CMR_{AK}$	IV A	N	N	4	2.35†
61*i=1	HLCI	Load CMR with A	$(A_b)\rightarrow CMR_{AK+100}$	IV A	N	N	4	2.35†
62	HLC	Shift Left Circularly	(A_a) Left Shifted End Around$\rightarrow A_a$	IV B	N	N	10	1.9†
63	HDLC	Shift Left Circularly Double	(A_{a+1}, A_a) Left Shifted End Around$\rightarrow A_{a+1}, A_a$	IV B	N	N	10	1.9†
64	HRZ	Shift Right Fill Zeros	(A_a) Right Shifted, Zero Fill$\rightarrow A_a$	IV B	N	N	10	1.9†
65	HDRZ	Shift Right Double, Fill Zeros	(A_{a+1}, A_a) Right Shifted, Zero Fill$\rightarrow A_{a+1}, A_a$	IV B	N	N	10	1.9†
66	HRS	Shift Right Fill Sign	(A_a) Right Shifted, Sign Fill$\rightarrow A_a$	IV B	N	N	10	1.9†
67	HDRS	Shift Right Double, Fill Sign	(A_{a+1}, A_a) Right Shifted Sign Fill$\rightarrow A_{a+1}, A_a$	IV B	N	N	10	1.9†
70 0	HSF	Scale Factor	Normalize (A_a) Shift Count$\rightarrow A_b$	IV A	N	N	5	3.1†
70 1	HDSF	Double Scale Factor	Normalize (A_{a+1}, A_a) Shift Count$\rightarrow A_b$	IV A	N	N	5	3.1†
70 2	HCP	Complement A	$(A_a)'\rightarrow A_a$	IV A	N	N	7	1.3†
70 3	HDCP	Double Complement A	$(A_{a+1}, A_a)'\rightarrow A_{a+1}, A_a$	IV A	N	N	7	1.3†
71 0	HOR	Logical Sum	$(A_a) \vee (A_b)\rightarrow A_a$; $(A_b)_H=(A_b)_H$	IV A	N	N	5	1.3†
71 1	HA	Sum	$(A_a) + (A_b)\rightarrow A_a$	IV A	N	N	5	1.3†
71 2	HAN	Difference	$(A_a) - (A_b)\rightarrow A_a$	IV A	N	N	5	1.3†
71 3	HXOR	Logical Difference	$(A_a) \bar{\vee} (A_b)\rightarrow A_a$	IV A	N	N	5	1.3†
71 5	HAND	AND	$(A_a) \odot (A_b)\rightarrow A_a$; $(A_b)_H=(A_b)_H$	IV A	N	N	5	1.3†
72***	—	Load IP BITE	(Other Processor CMR)$\rightarrow$CMR57	IV A	N	N	—	10.0†
73***	—	Store IP BITE	(CMR 57)$\rightarrow$Other Processor CMR	IV A	N	N	—	10.0†
74 0	HM	Multiply Register	$(A_a) \bullet (A_b)\rightarrow A_{a+1}, A_a$	IV A	N	N	5	12.1†
74 1	HD	Divide Register	$(A_{a+1}, A_a) \div (A_b)\rightarrow A_a$; Remainder$\rightarrow A_{a+1}$	IV A	N	N	5	12.1†
74 2	HRT	Square Root	$\sqrt{(A_{a+1}, A_a)}\rightarrow A_b$; Residue$\rightarrow A_{b+1}$	IV A	N	N	5	21.1†
74 3	HLB	Load B_x with B_b	$(B_b)\rightarrow B_x$	IV A	N	N	5	1.75†
74 4	HC	Compare, Register	Compare (A_a) to (A_b), Set CD	IV A	N	N	5	1.3†
74 5	HCL	Compare Limits, Register	If $(A_{a+1}) > (A_b) > (A_a)$, Set CD WITHIN	IV A	N	N	5	1.9†
74 6	HCM	Compare Masked, Register	Compare $(A_{a+1}) \odot (A_a)$ to (A_b), Set the CD	IV A	N	N	5	1.3†
74 7	HCB	Compare B_b with B_x	Compare (B_b) to (B_a), Set the CD	IV A	N	N	5	2.05†
77 0**	HSIM	Store IOC Monitor Clock in A	$(IOC_a$ MON CLK$)\rightarrow A_b$	IV A	N	N	5	3.8†
77 1	HSTC	Store Real-Time Clock in A	$(IOC_a$ RTC$)\rightarrow A_b$	IV A	N	N	5	3.8†
77 4*	HPI	Prevent Class III Interrupts	Set Class III Interrupt Lockout	IV A	N	N	9	1.3†
77 5*	HAI	Allow Class III Interrupts	Clear Class III Interrupt Lockout	IV A	N	N	9	1.3†
77 6*i=0	HALT	Stop Processor	Stop CPU	IV A	N	N	9	2.5†
77 6*i=1	HWFI	Wait for Interrupt	Cease Memory References until Interrupted	IV A	N	N	9	2.5†
77 6***i=1 a=1	—	Allow IP BITE	Allow IP BITE until Interrupted	IV A	N	N	—	2.5†

ULTRA/32 PSEUDO INSTRUCTIONS

10	ZA	Clear A	$0\rightarrow A_a$	I	N	Y	7	1.3
20	ZB	Clear B	$0\rightarrow B_a$	I	N	Y	7	2.35
20	NOOP	No Operation	$0\rightarrow B_0$	I	N	Y	9	2.35
23	SZ	Store Zeros	$0\rightarrow Y$	I	Y	Y	12	1.7
74 3	HNO	Half Word No Operation	$(B_0)\rightarrow B_0$	IV A	N	N	9	1.75†

ULTRA/32 FORMATING MNEMONICS

—	HK	Half Word Constant (Variable field becomes next halfword)	—	—	—	16	—
—	IW	Indirect Word (c=10)	—	—	—	8	—
—	IWS	Indirect Word, Special Base (c=00, c_1=0)	—	—	—	11	—
—	IWB	Indirect Word, Special Index (c=00, c_1=1)	—	—	—	11	—
—	IWC	Indirect Word, Character (c=01)	—	—	—	14	—
—	IWCI	Indirect Word, Character Increment (c=11)	—	—	—	14	—
—	MP	Memory Protection (see SPR format)	—	—	—	15	—

ULTRA/32 CODING FORMATS (UF) (An Asterisk (*) Preceding y Indicates Indirect Addressing)

No.	Variable Field	No.	Variable Field	No.	Variable Field	No.	Variable Field	No.	Variable Field
1	a, y, k, b, s	4	af_t, b	7	a	10	a, m (shift by m)	11	sy, b
2	a, y, b, s	5	a, b	8	y, b, s		a, b, 1 (shift by B_b)	12	y, k, b, s
3	ak, y, b, s	6	a, sy, b	9	None		a, b, 2 (shift by A_b)	13	sy, k, b

No.	Variable Field
14	y, w, p, b, s
15	r, i, or, ow, ia, ir
16	e

*Privileged **CPU→IOC Instr; —Privileged √Privileged when ak=2X, 5X, 6X or 7X ***Machine Language Only—Privileged

†Execution time independent of overlap operation

‡Times shown assume 750 ns memory with operands not in same 32K unit as instructions (overlapped).

I/O CONTROLLER COMMANDS

Code	Mnemonic	NAME	DESCRIPTION	UF**	Time μs
01	KECM	Load Control Memory	$(Y)\rightarrow CMR_{a|_j}$	1	4
02	KSCM	Store Control Memory	$(CMR_{a|_j})\rightarrow Y$	1	4
03	KSB	Set Bit I_j	$I\rightarrow Y_{I_j}$	2	6
04	KCB	Clear Bit I_j	$0\rightarrow Y_{I_j}$	2	6
05	KTB	Test Bit I_j	Sense Y_{I_j}; skip if $(Y_{I_j})=(u_{24})$	3	4
06	KTSB	Test and Set Bit I_j	Sense Y_{I_j}; skip if $(Y_{I_j})=0$; Set Y_{I_j}	2	6
07	KJ	Jump to Y	Y→Program Address Counter	4	2
10	KIB	Initiate Input Buffer on CI_j	$(Y)\rightarrow CMR$; (u)=Unit; (i_j)=Channel	5	4
11	KOB	Initiate Output Buffer on CI_j	$(Y)\rightarrow CMR$; (u)=Unit; (i_j)=Channel	5	4
12	KEFB	Initiate External Function Buffer on CI_j	$(Y)\rightarrow CMR$; (u)=Unit; (i_j)=Channel	5	4
13	KEIB	Initiate External Interrupt Buffer on CI_j	$(Y_{18:0})\rightarrow CMR$; (SMR)=Units; (i_j)=Channel	6	4
14	KIBF	Initiate Input Buffer on CI_j with Force	$(Y)\rightarrow CMR$; (j_a)=Channel	7	4
15	KOBF	Initiate Output Buffer on CI_j; with Force	$(Y)\rightarrow CMR$; (u)=Unit; (i_j)=Channel	5	4
16	KFBF	Initiate External Function Buffer on CI_j with Force	$(Y)\rightarrow CMR$; (u)=Unit; (i_j)=Channel	5	4
17	KTDB	Terminate Data Buffer on C_j	(j)=Channel; terminate Data Buffer	8	2
20	KTEI	Terminate External Interrupt Buffer on C_j	(j)=Channel; terminate EI Buffer	8	2
21	KI	Initiate Interrupt on C_j	Interrupt CP; $(_{ej})\rightarrow ISC$	5	2
22	KSBX	Store BITE on C_j	(BITE C_j)$\rightarrow Y$; (j_a)=Channel	7	4
23	KEDB	Enable/Disable BITE on CY	(u)=1-enable; (u)=0-disable; (Y)=Channels	9	4
24	KESM	Load External Interrupt Scan Mask on C_j	$(Y_{7:0})\rightarrow$Scan Mask; (j_a)=Channel	7	4
25	KSSM	Store External Interrupt Scan Mask on C_j	(Scan Mask C_j)$\rightarrow Y$	7	4
26	KSBS	Store Buffer Status on C_j	$(BCW_{31:0})\rightarrow Y_{+1}$; $(BCW_{59:32})\rightarrow Y$	7	6
27	KRB	Resume Buffer on C_{I_j}	$(Y)\rightarrow BCW_{59:32}$; $(Y_{+1})\rightarrow BCW_{31:0}$	6	6
30	KRCH	Release Channel Hold on C_j	(j_a)=Channel	8	2
31	KRTC	Load Real Time Clock	$(Y_{31:16})\rightarrow RTC_{31:16}$; $177777\rightarrow RTC_{15:0}$	4	4

FORMATING MNEMONICS

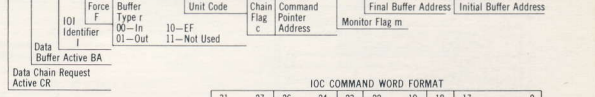
—	KBCW	Buffer Control Word	10 —

**ULTRA FORMAT

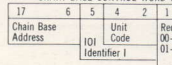
CMR—Control Memory Register
ISC—Interrupt Status Code
SCM—Scan Mask Register

1—$u|_{I_j}$, y, c
2—I_j, y, c
3—I_j, y, u, c
4—y, c
5—I, y, j, u, c
6—I, y, j, c
7—y, j, c
8—j, c
9—y, u, c
10—y, I, m (I=buffer length) (m=monitor)

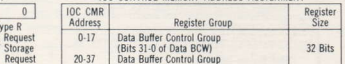
DATA BUFFER CONTROL WORD FORMAT



EI BUFFER CONTROL WORD FORMAT



IOC COMMAND WORD FORMAT



CHAIN BASE CONTROL WORD FORMAT

IOC CONTROL MEMORY ADDRESS ASSIGNMENT

IOC CMR Address	Register Group	Register Size
0-17	Data Buffer Control Group (Bits 31-0 of Data BCW)	32 Bits
20-37	Data Buffer Control Group (Bits 59-32 of Data BCW)	28 Bits
40-57	External Interrupt Buffer Control Group	19 Bits
60-77	Chain Base Control Group	12 Bits

INTERRUPT STATUS CODES

Class	INTERRUPT	Status Code Bits** 12 11 10 9 8 7 6 5 4 3 2 1 0
I*	Power Tolerance (Never Locked Out)	0 0 0 0 0 0 1 0 0 0
I	CP—Operand Memory Resume	0 0 M M M M M 0 0 0
I	CP—IOC Command Resume	K 0 0 0 0 0 0 0 0 1
I	CP—Instruction Memory Resume	0 0 M M M M M 0 0 1 0
I	CP—IOC Interrupt Code Resume	K 0 0 0 0 0 0 0 1 1
I*	Memory Parity Error	0 0 M M M M M 1 0 0 1
I*	IOC Memory Resume	K 0 M M M M M 1 0 1 0
I*	IOC Illegal CAR Command/Instruction	K 0 0 0 P W 1 0 1 1
I*	IOC Illegal Chain Command	K T C C C C 1 1 F F
II*	Interprocessor Interrupt	0 0 0 0
II	Floating Point Error	0 0 0 1
II	CP Illegal Instruction Error	0 0 1 0
II	Privileged Instruction Error	0 0 1 1
	Not Assigned	0 1 0 0
II	Operand Breakpoint Match	0 1 0 1
II	Operand Read or Indirect Addressing	0 1 1 0
	Not Assigned	0 1 1 1
	Not Assigned	1 0 0 0
II	Operand Write	1 0 0 1
II	Operand Limit	1 0 1 0
II	Instruction Breakpoint Match	1 0 1 1
	Not Assigned	1 1 0 0
II	Instruction Execute	1 1 0 1
II	Instruction Limit	1 1 1 0
II*	CP Monitor Clock	1 1 1 1
III*	IOC Monitor Clock	0 0 0 K 0 0 0 0 1 0 0 1
III*	IOC Illegal Buffer Initation	0 0 0 K T C C C C 1 0 1 0
III*	IOC—CP Interrupt	U U U K T C C C C 1 0 1 1
III*	IOC External Interrupt Monitor	U U U K T C C C C 1 1 0 0
III*	IOC External Function Monitor	0 0 0 K T C C C C 1 1 0 1
III*	IOC Output Data Monitor	0 0 0 K T C C C C 1 1 1 0
III*	IOC Input Data Monitor	0 0 0 K T C C C C 1 1 1 1
IV	Executive Return	16 bit code assigned thru program

*Queued

**Definitions: MMMM—16K Memory Banks (0-17); CCCC—IOI Channel (0-17); UUU—Peripheral Unit (0-7); W-0-Illegal IOC Command; I-Illegal CP-IOC Instruction; P—CP (0, 1); K—IOC (0, 1); T—IOI (0, 1); FF—Function: 00—Data Chain, 01—Error Chain, 10—"IOI" Chain, 11—Not Used

MEMORY PROTECTION REGISTERS

Storage Protection Register (SPR)

20	19	18	17	16	15	0
I	OR	OW	IA	IR	R	

- Displacement Value
- Allow use of Interrupt Index and Base Registers*
- Allow Indirect Addressing*
- Allow Operand Writing*
- Allow Operand Reading*
- Allow Instruction Execution*

*Operation Allowed if Bit is Set

SEGMENT IDENTIFICATION REGISTER (SIR)

20	19	17	16	15	0
	SIR_s			SIR_d	

- 16 Bit Displacement
- Base Register Designator

BREAKPOINT REGISTER

19	18	17 Comparison Address Bits	0
0	0	—Disabled	
0	1	—Instruction address	
1	0	—Operand address	
1	1	—Instruction and operand addresses	

CENTRAL PROCESSOR CONTROL MEMORY ADDRESS ASSIGNMENT

Task Mode

Address	Use	Bits
0-7	Accumulator (A) registers 0-7	32
10	Unassigned	19
11-17	Index (B) registers 1-7	19†
20-27	Base (S) registers 0-7**	18
30-47	Unassigned (not usable)	—

Interrupt Mode

Address	Use	Bits
50	Power Status Register**	32
51	Functional Status Register**	32
52-56	Unassigned (not usable)	—
57	Interprocessor BITE Storage**	32
6x	Breakpoint register**	20
7x	Active status register**	21
100-107	Accumulator (A) registers 0-7	33
110	CP monitor clock register	19*
111-117	Index (B) registers 1-7	19†
120-127	Base (S) registers 0-7	18
130-137	Unassigned (not usable)	—
140	ICW—Class I	20
141	DSW—Class I ASR storage	20
142	DSW—Class I interrupt status code	20
143	DSW—Class I P—storage	20
144	ICW—Class II	20
145	DSW—Class II ASR storage	20
146	DSW—Class II interrupt status code	20
147	DSW—Class II P—storage	20
150	ICW—Class III	20
151	DSW—Class III ASR storage	20
152	DSW—Class III interrupt status code	20
153	DSW—Class III P—storage	20
154	ICW—Class IV	20
155	DSW—Class IV ASR storage	20
156	DSW—Class IV interrupt status code	20
157	DSW—Class IV P—storage	20
160-167	Storage Protection Registers (SPR) 0-7	21
170-177	Segment Identification Registers (SIR) 0-7	21

*Clock is 16 Bits

**Not Addressable in the Task Mode.
(Privileged instruction error will occur)

†Lower 16 bits used for index and arithmetic functions. Upper three bits used **only** as a base-register designation.

ACTIVE STATUS REGISTER

Bit	Designator
20	Central Processor Identifier—Hardwired
19	State I (Hardware Control)
18	State II (Hardware Control)
17	State III (Hardware Control)
16	State IV (Hardware Control)
15	Upper—lower (Hardware Control)
14	Class I lockout
13	Class II lockout
12	Class III lockout
11	Base (S) register selector
10	Accumulator /B register selector
9	Memory lockout inhibit
8	Load base enable
7	Bootstrap mode
6-4	Usable spare bits
3	Fixed point overflow indicator
2	0—Not equal 1—Equal
1	0—Less than 1—G.T. or equal
0	0—Within limits 1—Outside limits

Bits 9-11 1—Interrupt mode
0—Task mode

FLOATING POINT FORMAT (each word is one's complement)

Sign Fill	±	14	0	±	30	0

Characteristic (exponent) in A_a or Y — Mantissa in A_{a+1} or Y_{+1}

INSTRUCTION WORD FORMATS

Format I

31	26	25	23	22	20	19	17	16	15	13	12	0
f		a		k		b		i	s			y

Format II

31	26	25	23	22	20	19	17	16	15	13	12	0
f		a		f_2		b		i	s			y

Format III

31	26	25	23	22	21	20	19	17	16	15	13	12	0
f		a		f_3	x	b		i	s			y	

Format IV A

31	26	25	23	22	20	19	17	16
15	10	9	7	6	4	3	1	0
f		a		f_4		b		i

Format IV B

31	26	25	23	22	16
15	10	9	7	6	0
f		a		m	

NORMAL INDIRECT ADDRESS WORD FORMAT

31	30	29	25	24	20	19	17	16	15	13	12	0
c		w		p		b		i	s			y

SPECIAL INDIRECT ADDRESS WORD FORMAT

31	30	29	28	20	19	17	16	15	0
c		c_1	x		b		i	d	

f—Function Code
f_2 f_3 f_4—Subfunction Codes
a—Accumulator Register
k—Operand Interpretation
b—Index Register
i—Indirect Bit

c_1—Special Indirect Subfunction
0—$Y=d+(S_b)$
1—$Y=d+(B_b)+(S)$ as specified by $(B_b)_{19\text{-}17}$

c—Addressing Designator
00—Indirect Special
10—Indirect Normal
01—Single Character
11—Sequential Character

s—Base Register
w—Field Width
p—Bit Position
y—Operand Address
x—Not Used
d—16 Bit Displacement

m—Shift Designator

Bit 26	Function
0	Shift by count 2^5—20
1	Shift by B_b if 2^5—0
1	Shift by A_b if 2^5—1

b is specified by bits 2^3—2^1

REPEAT CONDITIONS

a	Non-Compare Instructions
0	Terminate if A ≠ 0
1	Terminate if A = 0
2	Terminate if A ≥ 0
3	Terminate if A < 0
4	Do not terminate
5	Terminate if (A) is even parity on write into memory
6	Terminate if (A) is odd parity on write into memory
7	Do not terminate

a	Compare Instructions
0	Terminate if CD set to ≠
1	Terminate if CD set to =
2	Terminate if CD set to >
3	Terminate if CD set to ≥
4	Terminate if CD set to <
5	Terminate if CD set to ≤
6	Terminate if CD set to outside limit
7	Terminate if CD set to within limit

FORMAT I INSTRUCTION k—FIELD INTERPRETATION

k	Memory to Arithmetic (Read)	Arithmetic to Memory (Store)
0	sysE+(B_b)→$A_{15\text{-}0}$ SE	Not I*
1	$(Y_{15\text{-}0})$→$A_{15\text{-}0}$ SE	$(A_{15\text{-}0})$→$Y_{15\text{-}0}$; $Y_{31\text{-}16}$—Un
2	$(Y_{31\text{-}16})$→$A_{15\text{-}0}$ SE	$(A_{15\text{-}0})$→$Y_{31\text{-}16}$; $Y_{15\text{-}0}$—Un
3	$(Y_{31\text{-}0})$→$A_{31\text{-}0}$	$(A_{31\text{-}0})$→$Y_{31\text{-}0}$
4	$(Y_{7\text{-}0})$→$A_{7\text{-}0}$ ZE	$(A_{7\text{-}0})$→$Y_{7\text{-}0}$; $Y_{31\text{-}8}$—Un
5	$(Y_{15\text{-}8})$→$A_{7\text{-}0}$ ZE	$(A_{7\text{-}0})$→$Y_{15\text{-}8}$; $Y_{31\text{-}16}$—Un $Y_{7\text{-}0}$—Un
6	$(Y_{23\text{-}16})$→$A_{7\text{-}0}$ ZE	$(A_{7\text{-}0})$→$Y_{23\text{-}16}$; $Y_{31\text{-}24}$—Un $Y_{15\text{-}0}$—Un
7	$(Y_{31\text{-}24})$→$A_{7\text{-}0}$ ZE	$(A_{7\text{-}0})$→$Y_{31\text{-}24}$; $Y_{23\text{-}0}$—Un

k—Field Interpretation for Replace Instructions:
Read Cycle—Same as memory to arithmetic.
Store Cycle—Same as arithmetic to memory. For Repeat, with b of repeat instruction not zero, Y will be modified by S_6 and not S_4 for store cycle.

SE—Sign Extended; ZE—Zero Extended; Un—Unchanged

SYMBOL DEFINITIONS

CMR—Control Memory Register
F—Format
CA—Character Addressable
R—Repeatable
DSW—Designator Storage Word
UF—Ultra Format
$(A)_n$—Contents of A, bit n
CD—Compare Designator
Y—Address formed by $y+(B_b)+(S_4)$
ICW—Initial Condition Word
OD—Overflow Designator
Y—Operand (Y) (Whole word or partial word) or Y, depending on k
∩—Logical product (AND)
⊕—Logical sum (Inclusive OR)
⊕̄—Logical difference (Exclusive OR)

C. DMTU AND I/O BITE DATA

DMTU COMMAND WORD

BIT	Meaning
0	Stop
1	Fast Speed
2	Reverse Direction
3	Write
4	Erase
5	Track Number (LSB)
6	Track Number
7	Track Number (MSB)
8	BITE Set

DMTU STATUS CODES

BIT	Meaning
0	No Tape Tension
1	BOT
2	EOT
3	Illegal Function
4	Read Parity Error
5	Power Supply Fail
6	Record Bias Fail
7	Motor Motion Fail
8-30	Unused
31	Interrecord Gap

I/O BITE STATUS BITS

BIT	Meaning
31	Error Request
30	Output Parity Error
29	Input Parity Error
28	Periph Data Trans Error
27	Illegal Response
26	Performance Monitor
25	Unit Code (MSB)
24	Unit Code
23	Unit Code (LSB)
22-0	Always Zero

DMTU LOGIC DESCRIPTION

Desig.	Logic	Jack	Function
A1	21358	J16	Tape Transport Cartridge (TTC)
A2			Not Used
A3	21071	J3	Line Receiver
A4	21074	J4	Input-Output Logic
A5	21077	J5	Data Transfer Control
A6	21080	J6	Tape Format Logic
A7	21083	J7	Shift Register
A8	21086	J8	Status Word Generator
A9	21089	J9	Master Clock Generator
A10	21092	J10	Read Amplifier
A11	21095	J11	Write Amplifier
A12	21098	J12	Erase Amplifier
A13	21101	J13	Motor Control
A14	21104	J14	Motor Driver Amplifier
A15		J15	Power Supply

D. CONTROL AND RESPONSE CODE DESCRIPTIONS

Computer Control Code	Peripheral Response Code	
	100	101
100 Interrupt Request	No Interrupt	36-bit Interrupt Word follows
101 Output Request	No Output	Type I & III: Send data, halt output transfer and request interrupt Type II: Send Buffer A data
110 Input Request	No Input	Type I & III: 36-bit Interrupt Word follows Type II: Buffer A Input Word follows
111 Forced Output	Illegal Response	Send data, halt output transfer and request interrupt
	110	111
100 Interrupt Request	Previous computer message failed parity check; no interrupt	Previous computer message failed parity check; 36-bit interrupt Word follows
101 Output Request	Type I & III: Send data Type II: Send Buffer B Data	Previous computer message failed parity check; no output halt output transfer
110 Input Request	Type I & III: Input word follows Type II: Buffer B Input Word follows	Previous computer message failed parity check; no input halt input transfer
111 Forced Output	Send data	Previous computer message failed parity check; send data halt output transfer

E. CP AND I/O CARDS

Card	Loc.	Unit	Function
~~1089~~	07A-~~09A~~	CP	NDRO
1100	01A		Real Time Clock
1105	06B-11B	IOC	Active Buffer Reg.
1111	01B-04B	IOC	Interrupt Reg., CPIR
1116	02A-03A	IOC	CPIR (Bits 0-15)
1121	40A-43A	CPC	Registers/CM (16-31)
1126	44A-47A	CPC	Registers/CM (Ø-15)
1130	48A-51A	CPC	Registers, CM, A Adders
1135	43B-46B	IOC	Control Mem/DIR (0-15)
1140	25A	CP	Clocks
1146	27A	CPC	Interrupt Control
1150	26A	CPC	Cons., Int., Func. Trans.
1155	21A-24A	CPA	Arith. Regs.
1160	38A-39A	CPA	Shift Matrix
1166	12B-~~13B~~	IOI	Shift Reg. CC/RC
1170	47B-50B ~~53B~~-54B	IOI	1 Chan. Int., Par. Int.
1175	51B	IOI	11-Chan. Interface
1180	52B	IOI	111-Chan. Interface
1190	28B-31B	IOI	11 Shift Reg.
1195	24B	IOI	Test Card
1206	54A	CPC	Memory Int. Cont.
1210	32A	CPC	Registers, Control
1215	31A	CPC	Control Logic
1220	30A	CPC	Control Logic
1225	29A	CPC	Control Logic
1230	53A	CPC	Control Logic
1235	52A	CPC	Control Logic
1240	33A	CPA	Shift Matrix Cont.
1246	29B-30B	IOI	11-Serial Control, CC/RC
1250	22B	IOI	I, II-Serial Control
1255	42B	IOC	Control Mem/DIR (16-19)
1261	39B	IOC	Control Mem/DIR (28-31)
1265	41B	IOC	Control Mem/DIR (18-23)
1270	40B	IOC	Control Mem/DIR (24-27)
1276	04A	IOC	Interrupt Control
1280	25B	IOI	III-Shift Reg. (0-19)
1295	28A	CPC	Control Logic
1325	26B	IOI	III-Shift Reg. (20-31)
1331	27B	IOI	II, III-Serial Control
1335	21B	IOI	III-Serial Control, CC/RC
1340	33B	IOC	Timing
1350	34B	IOC	Control
1356	32B	IOC	Memory Control
1360	16A	CPA	Sequence Control
1365	17A	CPA	Arithmetic Control
1370	15A	CPA	Arithmetic Control
1375	14A	CPA	Arithmetic Control
1380	13A	CPA	Arithmetic Control
1385	12A	CPA	Arithmetic Control

7321890

CP — NDRO

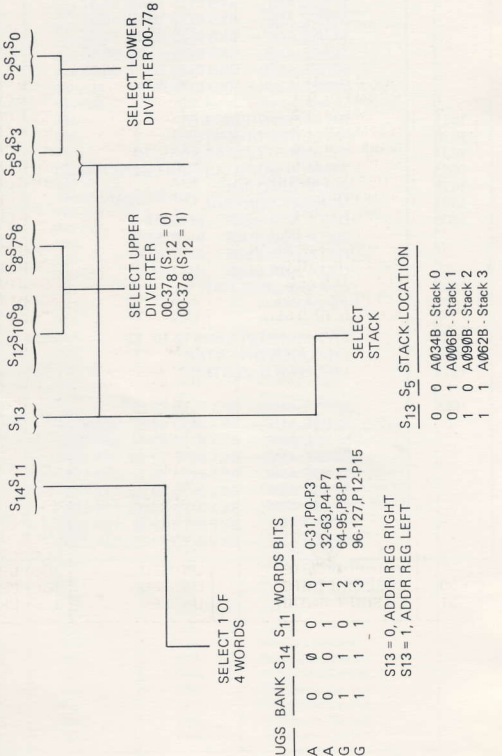
I/O

1881	15B	IOI	HARPOON Serial
1885	52B	IOI	HARPOON DISCRETE

F. MEMORY CARDS

1685	SENSE AMP – BK0 BITS 0-3, 32-35	001A
	SENSE AMP – BK0 BITS 4-7, 36-39	004A
	SENSE AMP – BK0 BITS 8-11, 40-43	007A
	SENSE AMP – BK0 BITS 12-15, 44-47	010A
	SENSE AMP – BK0 BITS 16-19, 48-51	013A
	SENSE AMP – BK0 BITS 20-23, 52-55	016A
	SENSE AMP – BK0 BITS 24-27, 56-59	019A
	SENSE AMP – BK0 BITS 28-31, 60-63	022A
	SENSE AMP – BK0 BITS P0-P7	025A
1611	RH UPPER DIVERTER	031A
1616	RH LOWER DIVERTER	034A
1631	RH ADR REQ/TRANS 0-10, 12	036A
1651	RH & LH WORD CURRENT GENERATOR	038A
1625	PULSE CONTROL	041A
1681	MEMORY CONTROL	048A
1605	DATA ADR BUSS BITS 0-7	050A
	DATA ADR BUSS BITS 8-15	052A
	DATA ADR BUSS BITS 16-23	054A
	DATA ADR BUSS BITS 24-31	056A
1640	CHANNEL CONTROL	058A
1620	PRIORITY	060A
1631	LH ADR REQ/TRANS 0-10, 12	067A
1616	LH LOWER DIVERTER	069A
1611	LH UPPER DIVERTER	071A
1685	SENSE AMP – BK1 BITS P8-P15	077A
	SENSE AMP – BK1 BITS 64-67, 96-99	080A
	SENSE AMP – BK1 BITS 68-71, 100-108	083A
	SENSE AMP – BK1 BITS 72-75, 104-107	086A
	SENSE AMP – BK1 BITS 76-79, 108-111	089A
	SENSE AMP – BK1 BITS 80-83, 112-115	092A
	SENSE AMP – BK1 BITS 84-87, 116-119	0954
	SENSE AMP – BK1 BITS 88-91, 120-123	098A
	SENSE AMP – BK1 BITS 92-95, 124, 127	101A

G. MEMORY ADDRESSING



H. MMCP REGISTER INDICATOR DESCRIPTIONS

BIT	CP ACCUM REG.	I/O CHAN REG.	I/O CHAN ENBL
0	NORM HOLD 0	INP BUF ACT	IOI-Ø CHAN 0 ACT
1	NORM HOLD 1	OUT BUF ACT	IOI-Ø CHAN 1 ACT
2	NORM HOLD 2	EF BUF ACT	IOI-Ø CHAN 2 ACT
3	NORM HOLD 3	FORCE ACT	IOI-Ø CHAN 3 ACT
4	NORM HOLD 4	EI BUF ACT	IOI-Ø CHAN 4 ACT
5	NORM HOLD 5	UNUSED	IOI-Ø CHAN 5 ACT
6	SHIFT CNT–NORM HOLD	101 CHN REQ	IOI-Ø CHAN 6 ACT
7	JUMP COND	ERR CHN REQ	IOI-Ø CHAN 7 ACT
8	REPEAT TERM	DATA CHN REQ	IOI-Ø CHAN 8 ACT
9	ACTIVE REPEAT	ERR CHN ENBL	IOI-Ø CHAN 9 ACT
10	ACTIVE CHAR ADDR	UNUSED	IOI-Ø CHAN 10 ACT
11	ERROR INT REQ	UNUSED	IOI-Ø CHAN 11 ACT
12	FLT PT DIV SEQ	DAT BUF REQ	IOI-Ø UNUSED
13	FLT PT MULT SEQ	EI BUF REQ	IOI-Ø UNUSED
14	ADD/SUB RND SEQ	UNUSED	IOI-Ø UNUSED
15	FLT PT ADD/SUB SEQ	CP INT REQ	IOI-Ø UNUSED
16	EARLY EXIT SEQ	EI MON REQ	IOI-Ø UNUSED
17	CHAR ADDR SEQ	DAT MON REQ	IOI-Ø UNUSED
18	COUNT ONES SEQ	INT ASN REG(I)	IOI-Ø UNUSED
19	DIVIDE SEQ	INT ASN REG(X)	IOI-Ø UNUSED
20	MULTIPLY SEQ	UNUSED	IOI-1 CHAN 20 ACT
21	DON'T CARE SEQ	UNUSED	IOI-1 CHAN 21 ACT
22	SQUARE ROOT SEQ	UNUSED	IOI-1 CHAN 22 ACT
23	SCALE SEQ	UNUSED	IOI-1 CHAN 23 ACT
24	SHIFT SEQ	UNUSED	IOI-1 CHAN 24 ACT
25	JUMP SEQ	UNUSED	IOI-1 CHAN 25 ACT
26	WRITE SEQ	UNUSED	IOI-1 CHAN 26 ACT
27	STORE SEQ	UNUSED	IOI-1 CHAN 27 ACT
28	READ SEQ	UNUSED	IOI-1 CHAN 28 ACT
29	INH SHIFT GATE	UNUSED	IOI-1 CHAN 29 ACT
30	ENBL SHIFT REG	UNUSED	IOI-1 CHAN 30 ACT
31	LD SHIFT MATRIX	UNUSED	IOI-1 CHAN 31 ACT

H. MMCP REGISTER INDICATOR DESCRIPTIONS (Continu

BIT	CP (CMR 050) POW STAT REG.	CP (CMR 051) FUNC. STAT REG.	CP REPEAT REG.
0	CP(I) BITE	PROC(1) BITE	0
1	SEC	CP TIME OUT	1
2	INT	WAIT INT	2
3	PRI	OVERTEMP	3
4	IO(I) BITE	BITE	4
5	SEC	NDRO PARITY	5
6	INT	8K INTER	6
7	PRI	SPARE	7
8	CP(X) BITE	PROC(X) BITE	8
9	SEC	CP TIME OUT	9
10	INT	WAIT INT	10
11	PRI	OVERTEMP	11
12	IO(X) BITE	BITE	12
13	SEC	NDRO PARITY	13
14	INT	8K INTER	14
15	PRI	SPARE	15
16	MEM 0 BITE	MEM 0 BITE	
17	SEC	MEM DISABLE	B-DESIG
18	INT	PARITY (BK0)	B-DESIG
19	PRI	PARITY (BK1)	B-DESIG
20	MEM 1 BITE	MEM 1 BITE	
21	SEC	MEM DISABLE	
22	INT	PARITY (BK2)	
23	PRI	PARITY (BK3)	A-DESIG
24	MEM 2 BITE	MEM 2 BITE	A-DESIG
25	SEC	MEM DISABLE	A-DESIG
26	INT	PARITY (BK4)	
27	PRI	PARITY (BK5)	
28	UNUSED	UNUSED	
29	UNUSED	UNUSED	
30	UNUSED	UNUSED	
31	UNUSED	UNUSED	Repeat Active

I. KEY TEST POINTS

BIT	FSR	PSR	ASR	POWER			
				Volt	Unit	TP	Conv
0	47A-11	47A-12	47A-07	GND	CPIO	01A-11	
1	47A-09	47A-05	47A-08	+28	CP	–	~~1200~~
2		47A-02	47A-10	-5.0	CP	28A-14	1300
3		47A-03	47A-13	-5.7	CP	25A-18	1300
4	46A-11	46A-12	46A-07	~~+6.7~~	CP	7A-15	1300
5	46A-09	46A-05	46A-08	+6.0	IO	~~47A-21~~	~~1300~~ 53B-21 1200
6	54A-19	46A-02	46A-10	~~+5.0~~ +6.1	IO	52B-22	1200
7	54A-17	46A-03	46A-13	-5.3	IO	52B-12	~~1300~~ 1200
8	45A-11	45A-12	45A-07	-5.7	IO	~~52B-26~~	1200 1A-6
9	45A-09	45A-05	45A-08	-10.	IO	~~47B-02~~	~~1300~~ 1200 54B-2
10		45A-02	45A-10				
11		45A-03	45A-13	GND	MEM	38A-14	1840
12	44A-11	44A-12	44A-07	+28.	MEM	–	1840
13	44A-09	44A-05	44A-08	+20.	MEM	38A-09	1840
14		44A-02	44A-10	+10.	MEM	38A-10	1840
15	54A-16	44A-03	44A-13	+6.0	MEM	38A-13	1840
16	43A-20	43A-12	53A-12	-6.0	MEM	38A-08	1840
17	43A-19	43A-23	53A-11	+5.0	MEM	38A-11	1840
18	43A-17	43A-22	53A-10				
19	43A-16	43A-21	53A-09	-10.	MEM	38A-12	1840
20	42A-20	42A-12					
21	42A-19	42A-23		All Units – If RTM Is Running 28V Is Present.			
22	42A-17	42A-22					
23	42A-16	42A-21					
24	41A-20	41A-12					
25	41A-19	41A-23					
26	41A-17	41A-22					
27	41A-16	41A-21					
28							
29							
30							
31							

1. Functional Prints

CP-7511100
10-7511100
Memory -7131678
MCP-7216601
MMCP-7094243

2. Card Prints (713XXXX)

1089	1170	1250	1365
1100	1175	1255	1370
1105	1180	1261	1375
1111	1185	1265	1380
1116	1190	1270	1385
1121	1195	1276	1605
1126	1206	1280	1611
1130	1210	1295	1616
1135	1215	1325	1620
1140	1220	1331	1625
1146	1225	1335	1631
1150	1230	1340	1640
1155	1235	1350	1681
1160	1240	1356	1685
1166	1246	1360	

3. Miscellaneous Drawings

MMCP	CP/IO	PWR SUP	DC/DC CONV
7511350	7131000	7131700	7511200
7094200	7131001	7131701	7511205
7094300		7131720	7511210
7094305		7131730	7511222
7094310	MEM	7131735	7511300
7094315		7131740	7511305
	7131500	7131780	7513140
MCP	7131501		7131806
		FRAME	7131780
7131300			7131785
7131305		7131832	
		7131833	

4. Wire Tabs (Dwg. No.)

7131983 - Cable (W1)
7131985 - Cable (W2)
7131981 - Cable (W3)
7131951 - Cable (W4)
7131963 - Cable (W5)
7131931 - Cable (W6)
7131941 - Cable (W7)
7131971 - Cable (W8)
7131991 - Cable (W9)
7131045 - CP Chassis (7131001-03)
7131580 - Mem Chassis (7131501-11)
7131567 - Mem Conn. Pnl (7131501-11)
7131568 - Mem Word Wir (7131501-11)
7131505 - Sense Cable (W1, 2, 3, 4)
7131507 - Sense Cable (W5, 6, 7, 8)
7511250 - Pwr. Sup. (7131701-06)
7511251 - Pwr. Sup. (7131701-07)
7131756 - Sw. Reg. (7131720)
7131757 - Sw. Reg. (7131740)
7511256 - FC/DC (7511200-01)
7511301 - DC/DC (7511300-01)
7511303 - DC/DC (7511300-01)
7511839 - DC/DC (7131840-00)

5. Parts list (For each drawing in Item 2 and Item 3 above.)

K. CP AND I/O MEMORY BUS RESISTANCE

Note: Add cabinet connectors for J1, J11, J21 & J2, J12, J22

CABINET CONNECTOR J39

REF. CABLE 7131930, TERM. BD. No. 2, CONNS. J2, 12, 22

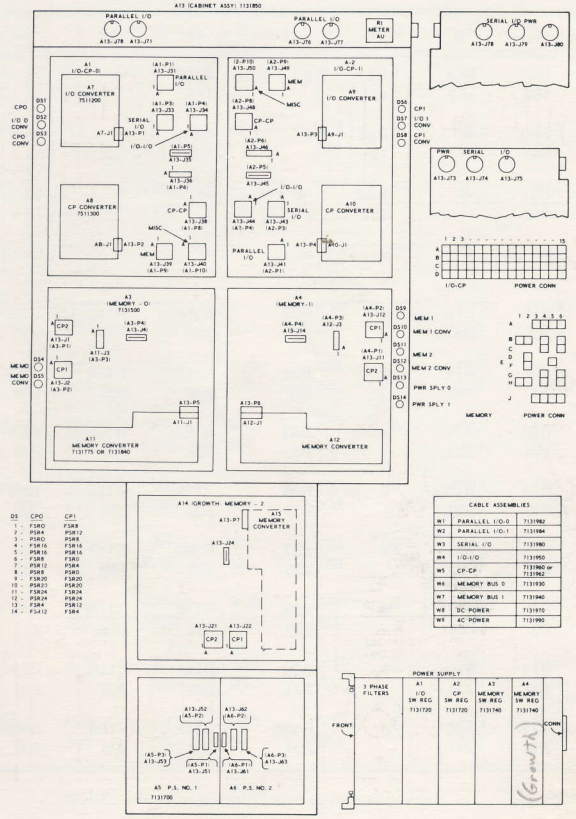
CABINET CONNECTOR J49

REF. CABLE 7131940, TERM. BD. No. 1, CONNS. J1, 11, 21

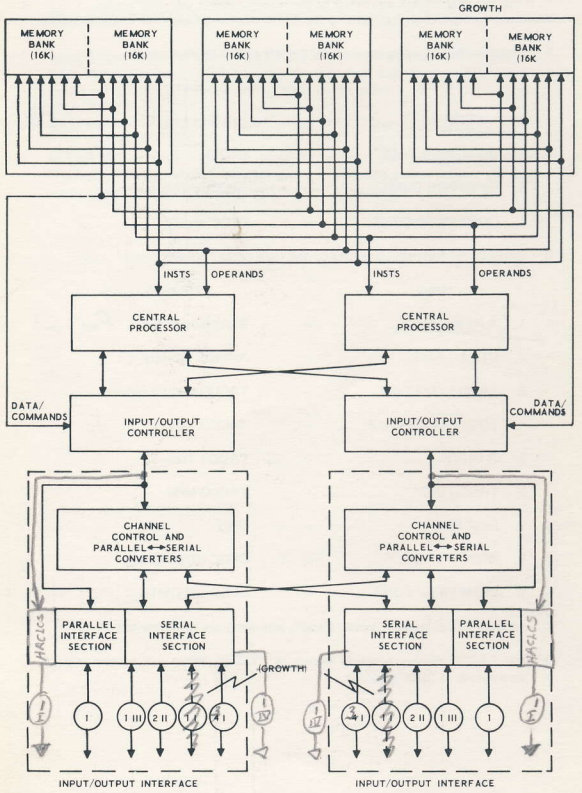
	1	2	3	4	5	6	7
A	R1 137	Ø	∞	∞	Ø	R41 121	∞
B	R2 137	Ø	∞	R22 221	Ø	R42 121	R43 162
C	∞	R3 162	∞	∞	∞	∞	R44 162
D	∞	∞	∞	R23 162	∞	∞	∞
E	R33 200	R5 200	R13 200	R25 200	∞	R45 200	R53 200
F	R37 200	R6 200	R14 200	R26 200	∞	R46 200	R54 200
G	R35 200	R7 200	R15 200	R27 200	Ø	R47 200	R55 200
H	R36 200	R8 200	R16 200	R28 200	Ø	R48 200	R56 200
J	R37 200	R9 200	R17 200	R29 200	Ø	R49 200	R57 200
K	R38 200	R10 200	R18 200	R30 200	Ø	R50 200	R58 200
L	R39 200	R11 200	R19 200	R31 200	Ø	R51 200	R59 200
M	R40 200	R12 200	R20 200	R32 200	Ø	R52 200	R60 200

8	9	10	11	12	13	14
R61 162	R64 162	R81 121	Ø	R101 162	∞	∞
R62 162	∞	R82 121	Ø	R102 162	∞	∞
R63 162	∞	R83 162	∞	∞	∞	∞
∞	∞	∞	∞	∞	∞	∞
R65 200	R73 200	∞	R93 200	R105 200	R113 200	R85 200
R66 200	R74 200	Ø	R94 200	R106 200	R114 200	R86 200
R67 200	R75 200	Ø	R95 200	R107 200	R115 200	R87 200
R68 200	R76 200	Ø	R96 200	R108 200	R116 200	R88 200
R69 200	R77 200	Ø	R97 200	R109 200	R117 200	R89 200
R70 200	R78 200	Ø	R98 200	R110 200	R118 200	R90 200
R71 200	R79 200	Ø	R99 200	R111 200	R119 200	R91 200
R72 200	R80 200	Ø	R100 200	R112 200	R120 200	R92 200

NOTE: All values are referenced to cabinet ground.
All tolerances are ±1%.



CABLE ASSEMBLIES		
W1	PARALLEL I/O-0	7131982
W2	PARALLEL I/O-1	7131984
W3	SERIAL I/O	7131980
W4	I/O-I/O	7131950
W5	CP-CP	7131960 or 7131962
W6	MEMORY BUS 0	7131930
W7	MEMORY BUS 1	7131940
W8	DC POWER	7131970
W9	AC POWER	7131990



(1I) HACLCS IOC_0-Ch. 11_8 IOC_1-Ch 31_8 (ONLY)

(1IV) HARPOON Ch. 10_8, Ch. 30_8 (either IOC)

Section 2
GPDC POWER UP PROCEDURE

Minimum configuration for running the GPDC diagnostic with the TACCO display.

A. Energize the following breakers on the left circuit breaker panel.

	Name		Function
1.	L XFMR RECT	–	Left Side of A/C for 28 vdc
2.	DGTL MAG TAPE	–	DMTU
3.	GPDC PWR SUPPL	–	GPDC (Left Side)
4.	COMPTR GP CONT	–	GPDC and DMTU

B. Energize the following breakers on the right circuit breaker panel.

	Name		Function
1.	R XFMR RECT	–	Right Side of A/C for 28 vdc
2.	INT AV FAN	–	Avionics Blowers
3.	TACCO CON FAN	–	TACCO Station Blowers
4.	LOGIC XFMR No. 2	–	TACCO Tray
5.	R INCOS	–	TACCO Tray
6.	TACCO DISP	–	TACCO MPD
7.	DISP GEN	–	DGU
8.	GPDC PWR SPLY	–	GPDC (Right Side)
9.	COMPTR GP CONT	–	GPDC and DMTU

C. At the TACCO station "Power Panel", put computer group switch up.

D. Put TACCO display function switch to "TEST". When test pattern appears, turn switch to "ON" position.

Section 3
AND EXECUTE THE GPDC DIAGNOSTIC WITH NO MMCP

1. Put a cassette into the DMTU. Press "RESTART" on the TACCO "POWER PANEL".

2. After 4 minutes max, the selection load cue should appear on the TACCO MPD. At this point – NDRO loaded the selection loader program, selection loader put up the cue and is waiting for parameter entry.

3. Depress numeric "3" and "ENTER" on the TACCO tray.

4. AFTER 90 seconds max. the alert "Program Load and Verification in Progress. ." should appear. At this point – selection loader loaded the test loader program and the GPDC diagnostic ran successfully.

Section 4
LOAD AND EXECUTE THE GPDC DIAGNOSTIC WITH MM

1. Connect the MMCP to CPØ. Put a cassette into the DMTU. Set Key 7 on the MMCP. Press "RESTART" on the TACCO "POWER PANEL".

2. After 3 minutes max a 7-step with P-3400306 should occur. At this point – NDRO loaded the selection loader program and got a good checksum.

3. Set Keys 3 and 6 on the MMCP. Press "START" on the MMCP.

4. A 6-stop with P-1000XXX should occur immediately. At this point – selection loader is waiting for a parameter entry.

5. Enter an octal 03 in CMR 100 on the MMCP. Put Keys 6 and 3 down on the MMCP. Press "START" on the MMCP.

6. After 30 seconds max a 7-stop with P-2000XXX should occur. At this point – selection loader loaded the test loader program – test loader loaded the GPDC diagnostic program – the GPDC diagnostic is ready to execute.

7. Set Key 6 and press "START" on the MMCP.

8. After 12 seconds max a 6-stop with P-0013044 should occur. At this point – CP1 ran the CP, memory, and I/O portion of the diagnostic – CP0 began the CP test and stopped in the Jump/Stop test.

9. Press "START" on the MMCP.

10. A 7-stop should immediately occur with P-0013045. At this point – CP0 is still in the Jump/Stop portion of the CP test.

11. Press "START" on the MMCP.

12. After 12 seconds a 7-stop with P-4016061. At this point – the 1832 has successfully completed the GPDC diagnostic.

Section 5
FAILURE ANALYSIS WITH NO MMCP

No selection load cue

1. Check the timers on the GPDC, DMTU, DGU, MPD and Keyset. If they are moving, each of these units have power.

2. Check the test pattern on the MPD. If it's bad, the display is down.

3. Check the DMTU BITE indicator. If it is set, NDRO failed to load on any of its sixteen load paths, passed a self-check test on the DMTU interface, and set the DMTU BITE indicator. Try swapping the cassette and run again.

4. Check the DGU BITE indicator. If it is set, the DGU sensed an internal failure and set the BITE indicator.

5. Check the GPDC BITE indicators.

   A. If MEM 1 is set and all others are clear, NDRO tried to "load and run" in memory 1 and a memory parity error occurred. Restart to try in memory Ø.

   B. If MEM Ø is set and all others are clear, NDRO tried to load and run in memory Ø and a memory parity error occurred. Try swapping memories and run again.

   C. If the CPØ, MEM Ø, and MEM 1 are set and all others are clear, NDRO failed to load on any of its sixteen load paths, failed a self-check test on the DMTU interface and set these indicators. Try swapping CP's and run again.

6. At this point no definite failure indications exist. If time permits, get the MMCP and start over. Otherwise try the following actions:

   A. Measure the DC voltages in the 1832 to see if any power supplies are bad.

   B. Check all of the I/O cables for security.

   C. Swap units in the following order: (cassette, DMTU, CP, memory, MPD, DGU).

No 7—stop after NDRO load from DMTU

1. Operating procedure

   A. Restart to 6 stop. Stop ALT CP.

   B. Set stop 7.
      Clear CMR 127.
      Set CMR 060 to 1000062.
      Set breakpoint switch to manual.

   C. Follow flowchart until alpha connector, Table 2 will identify cause of load failure.

2. Load failure identification table

   A. DMTU status error. See (S6+42) for DMTU status word.
      Status word format
      BIT 0 No Tape Tension
      BIT 1 BOT
      BIT 2 EOT
      BIT 3 Illegal Function Code
      BIT 4 Read Parity Error
      BIT 5 Power Supply Failure
      BIT 6 Record Bias Failure
      BIT 7 Motor Motion Failure
      BIT 31 IRG (0-DATA)

   B. Unexpected Class 111 interrupt received. Suspect IOC problem.

   C. No BOT status for 10 seconds after rewind EF sent. i.e., BIT 01 clear in each status word received.

   D. No interrupts received for 10 seconds after rewind is sent.

   E. IRG status received in all status words for 10 seconds after read EF sent. (Suspect no data on tape.)

   F. No interrupts received for 10 sec. after read EF sent.

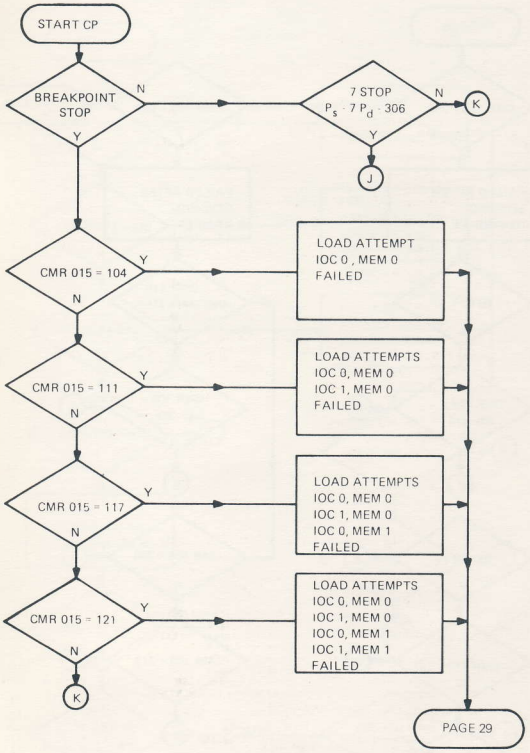
   G. No input data received for 1 sec. after "DATA" status received.

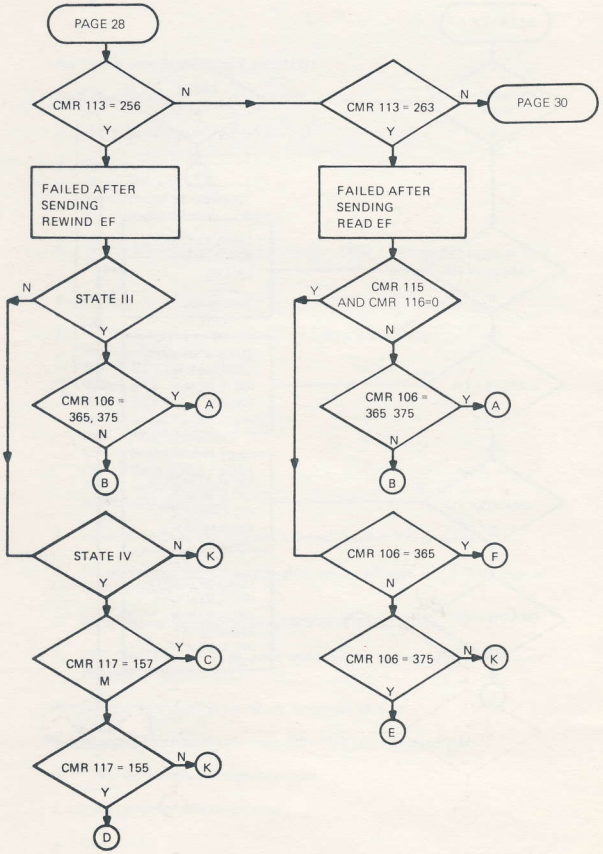
   H. "101" or error chain run during input.

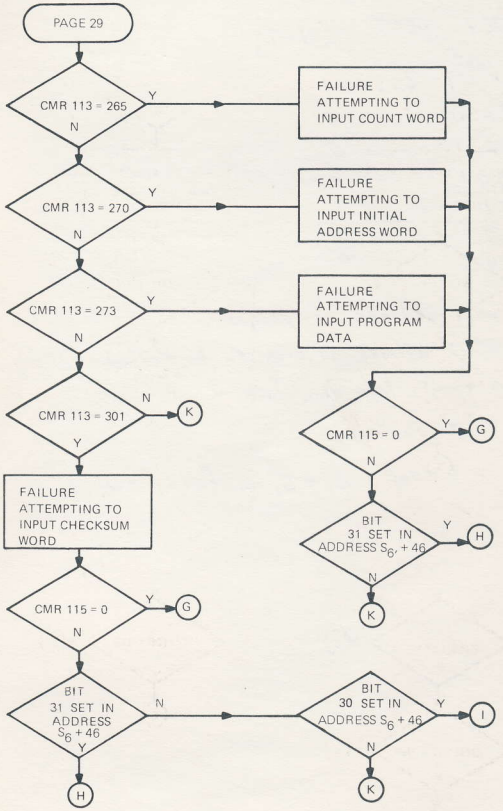
   I. Input complete. Checksum error.

   J. Good load.

   K. NDRO related problem.




PAGE 28
CMR 113 = 256
N
Y
CMR 113 = 263
N
Y
PAGE 30
FAILED AFTER SENDING REWIND EF
FAILED AFTER SENDING READ EF
STATE III
N
Y
CMR 115 AND CMR 116=0
Y
N
CMR 106 = 365, 375
Y
N
A
B
CMR 106 = 365 375
Y
N
A
B
STATE IV
N
Y
K
CMR 106 = 365
Y
N
F
CMR 117 = 157 M
Y
C
CMR 106 = 375
N
Y
K
E
CMR 117 = 155
N
Y
K
D


PAGE 29
CMR 113 = 265
Y
N
FAILURE ATTEMPTING TO INPUT COUNT WORD
CMR 113 = 270
Y
N
FAILURE ATTEMPTING TO INPUT INITIAL ADDRESS WORD
CMR 113 = 273
Y
N
FAILURE ATTEMPTING TO INPUT PROGRAM DATA
CMR 113 = 301
N
Y
K
CMR 115 = 0
Y
N
G
FAILURE ATTEMPTING TO INPUT CHECKSUM WORD
BIT 31 SET IN ADDRESS S_6 + 46
Y
N
H
K
CMR 115 = 0
Y
N
G
BIT 31 SET IN ADDRESS S_6 + 46
N
Y
BIT 30 SET IN ADDRESS S_6 + 46
Y
N
I
H
K

Check Memory bits:

Use 11 Inst. (Load A & Index B)
CLR S_0
CLR Bit 14 in ASR
CLR B_1
START

MEMORY TEST (short)

0	611111	622001
1	242311	0
2	442311	0
3	5301	6
4	5211	1
5	5373	0
6	5343	4

S_0 = base address of program
S_1 = start address of area to be tested (10_8)
A_1 = a count less than 100K
A_2 = Test Pattern
error - 4-stop, B_1 + S_1 is failing address