OPERATING INSTRUCTIONS FOR DEBUG MODULE

COMMON PROGRAM DEBUG FUNCTIONS

Retrieve Base Address
DB ABS MN S V/
(DF: S, V = 0)

Authorize Debug for Write Access*
DB AUTH MN_1 S_1 MN_2 S_2 . . . MN_n S_n/
(DF: All Modules)

Change Several Words Incrementally
DB CHNG ADR_1 DATA C NTND K/
(DF: C = 3; NTND, K = 1)

Clear Previous Debug Requests
DB CLR X/
(DF: X = 0)

Calculate Duty Cycle
DB CYCL ADR_1 ADR_2 NX PCBEX D/
(DF: NX = 1; PCBEX, D = 0)

Perform Immediate Memory Dump
DB DUMP ADR_2 ND K D/
(DF: ND, K = 1; D = 0)

Dump Backlog Table*
DB DBKL L/
(DF: L = 0)

Provide Time History
DB HIST ADR_1 ADR_2 NT PCBEX D/
(DF: NT = 1; PCBEX, D = 0)

Inspect Memory (and Backlog Changes*)
DB IAC(B) ADR_1 F/
(DF: F = 1)

Change Inspected Address
DB C DATAWD/

Display Next Sequential Address
DB N/

OPERATING INSTRUCTIONS FOR DEBUG MODULE

COMMON PROGRAM DEBUG FUNCTIONS

Terminate Active Inspect and Change Function*
DB T/

Trap Intermodule Message
DB IMSG MN MT N D/
(DF: N = 1; D = 0)

Initialization
DB INIT MN_1 S_1 V_1 $OFFSET_1$ MN_2 S_2 V_2 $OFFSET_2$/
(DF: All fields = 0 for absolute debugging)

Send Intermodule Message
DB MGTR MN MT W_1 W_2 . . . W_{12}/

Present Module History
DB MODH MN E DC D/
(DF: E, DC, D = 0)

Repeat Debug Requests
DB RPT NT RP/
(DF: NT = 1; RP = 0)

Search Memory For Constant
DB SCON ADR_1 ADR_2 SCHDATA MSK D/
(DF: MSK = 37777777777; D = 0)

Sequence Debug Requests
DB SEQ INC NT
(DF: INC, NT = 1)

Present Contents of Registers and Memory
DB SNAP ADR_1 N BSA ADR_2 ND K PCBEX D/
(DF: N, ND, K = 1; BSA, ADR_2, PCBEX, D = 0)

Perform Operand Search
DB SOPR ADR_1 ADR_2 SCHOPR NT D/
(DF: NT = 1; D = 0)

Calculate Time of Execution
DB TIME ADR_1 ADR_2 NX PCBEX D T/
(DF: NX = 1; PCBEX, D, T = 0)

*Executed from I/O Console only

DEBUG MODULE FUNCTION DEFINITIONS

DF – Defaulted. A field value assumed by the Debug Module without requiring an operator type-in. May not be followed by a non-defaulted field.

ADR – Address (5 digit maximum)

BSA – Selective Register Word
A = All accumulators; B = All Index Registers
S = All Base Registers; 0 = No Registers Dumped

C – Code for Data Storage Format
1 – Lower Half Word
2 – Upper Half Word
3 – Whole Word
4 – K_4 (0–7)
5 – K_5 (8–15)
6 – K_6 (16–23)
7 – K_7 (24–31)

D – Device
0 = Output to Input Device
1 = Paper Tape I/O CSL 1
2 = Paper Tape I/O CSL 2

DATA – Whole, Half, or Quarter Word based on C.

DATAWD – Data Word. Same format as in IAC or IACB.

DC – Duty Cycle
0 = No Duty Cycle
1 = Duty Cycle

E – Entrance Type History
0 = All
1 = Priority
2 = Message
3 = Periodic
4 = Deferred
5 = Demand
6 = I/O Interrupt

F – Format
W = Whole Word Data
H = Half Word Data
Q = Quarter Word Data
I = Instruction

INC – Increment to Base Address

K – Increment if Data Changed at Several Locations or for Non-Continuous Memory

DEBUG MODULE FUNCTION DEFINITIONS

L – Segment Link
0 = No Segment Link Code punched on Paper Tape
1 = Segment Link Code punched on Paper Tape

MSK – Mask (Inclusive OR)

MN – Module Mnemonics at I/O Console
Module Number at UYA-4 Console.

MT– Message Type
0 = All messages to MN are trapped

N – Number of SNAPs or Number of Messages to Trap

ND – Number of Words to Dump

NT – Number of Times (13_8 max.)

NX – Number of Times Measurement is Taken (377_8 max.)

NTND – Number of Times New Data is Entered

OFFSET – Relative Offset to MN, S, V

PCBEX – Pass Count Before Execution

RP – Repetition Period in Hundredths of Seconds

S – Segment Number

SCHDATA – Number to Search For

SCHOPR – Operand to Search For

T – Max. and Min. Time Output
0 = No output
1 = Output

V – Version Number

W_1– W_{12} – Octal Data Words of Intermodule Message
W_i Formats:
Whole word = data
Half word = data, data
Quarter word = data, data, data, data

X – 0 = Clear Last Debug Request
2 = Clear Previous Debug Requests
4 = Clear All Authorizations