AN/UYK-7(V) DIAGNOSTIC SUPPLEMENTARY TESTS

A0 = IOC No.
A1 = Normal Output
A2 = I Bus Test Selected Memory Banks
A3 = 0 Bus Test Selected Memory Banks
A4 = Channels-To-Test
A5 = ESA Channel-To-Test
A6 = Banks-To-Test
A7 = Subtest Select
S1 = Load Bias
P = 0200 + S1

	A7 Bit	Subtest Selected	Selectable Registers
Manual	0	Power Loss	See Para. 4.23.3.2
	1	CP Panel	See Para. 4.23.3.3
	2	Bootstrap Auto Recovery	See Para. 4.23.3.4
	3	Auto Start	See Para. 4.23.3.5
	4	IOC Panel	See Para. 4.23.3.6
	5	Power Fluctuation	See Para. 4.23.3.7
Unused	6		
	7		
Single-CPU	8	AEGIS Single Bus	A0, A1, A2, A3, A7, S1, P
	9	Memory O Bus Fasthit	A0, A1, A3, A7, S1, P
	10	Privileged Interrupt Error	A0, A7, S1, S2, S3, P
	11	IOC Memory Bank Addressing	A0, A6, A7, S1, P
	12	Double Density Memory Disturb	A6, A7, S1, P
	13	IOC Clock	A0, A7, S1, P
	14	End-Around Channel	See Para. 4.23.4.7
	15	End-Around Multi-Intercomputer	See Para. 4.23.4.8
	16	ESI Channel	A0, A4, A7, S1, P
	17	ESA Input	A0, A1, A5, A7, S1, P
	18	ESA Output	A0, A5, A7, S1, P
	19	CDM (Continuous Data Mode)	A0, A1, A7, S1, P
	20	IOC Addressing	A0, A7, S1, P
	21	CPU Memory Addressing	A6, A7, S1, P
Multi-CPU	22	Memory Access	See Para. 4.23.5.1
	23	IOC O Bus Noise	See Para. 4.23.5.2
	24	IPI (Inter-Processor Interrupt)	See Para. 4.23.5.3
	25	IOC Interface	See Para. 4.23.5.4
	26	Memory O Bus Noise	See Para. 4.23.5.5
	27	Memory Interface	See Para. 4.23.5.6
	28	Interrupt Generator	See Para. 4.23.5.7
	29	IOC Interrupt Lockout	See Para. 4.23.5.8
	30	Memory Z Register Noise	See Para. 4.23.5.9
	31	Power Interrupt	See Para. 4.23.5.10

Key Options

Jump 1
Jump 2
Jump 3
Stop 4
Stop 5
Stop 6
Stop 7 Ending address for all tests at 6 Stop is P = 400346 (S1 + 346)

ABBREVIATED OPERATING INSTRUCTIONS FOR AN/UYK-7(V) COMPUTER DIAGNOSTICS

(REFER TO NAVSEA 0967-024-5453 PART 1, 2, 3, CHANGE 5)

Bootstrap Load

A3 = Load Channel
S1 = Load Bias
S6 = Bias + 37700

CPU Diagnostic (2 seconds)

A0 = IOC No.
S1 = Load bias
P = 0 + S1

IOC/IOA Diagnostic (25 seconds)

A0 = IOC No.
A1 = Channels to Test
A2 = IC Channels to Test (Must Also Be Selected in A1)
A3 = End-Around-Channels to Test (Must Also Be Selected in A1)
S3 = 20,000 + Load Bias
P = 0 + S3

Memory Diagnostic (Core Memory 25 Seconds Per Module, DDMFM 2 minutes Per Module)

A0 = IOC No.
A6 = Banks to Test (Bits 0-15 For Core, Bits 16-31 For DDMFM)
A7 = Memory Options
Bit 31 - Bypass 1 Bus
Bit 30 - Bypass Pattern Tests
S2 = 30,000 + Load Bias
P = 0 + S2

Key Options

Jump 1 = Interleaved Core Memory
Jump 2 = End-Around-Channels
Jump 3 = Loop On Diagnostic
Stop 4 = Unexpected Class I Interrupt
Stop 5 = Error Stop
Stop 6 = End of Individual Diagnostic
Stop 7 = End of Individual Subtest

Ending Addresses

Separated Tests

CPU = 411303 (S1 + 11303)
IOC = 7000 (S0 + 7000)
MEM = 1000122 (S2 + 122)

Confidence Test

CPU = 411303 (S1 + 11303)
IOC = 7000 (S0 + 7000)
MEM = 2000122 (S4 + 122)

Confidence Test

A0 = IOC No.
A1 = Channels to Test
A2 = IC Channels (Must Also Be Selected in A1)
A3 = End-Around-Channels (Must Also Be Selected in A1)
A6 = Banks to Test (Bits 0-15 For Core, Bits 16-31 For DDMFM)
A7 = Memory Options
Bit 31 = Bypass 1 Bus
Bit 30 = Bypass Pattern Tests
S1 = Load Bias
P = S1 + 17770