

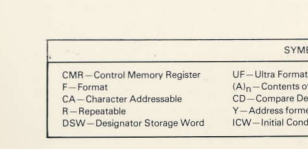
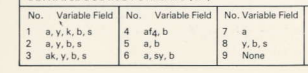
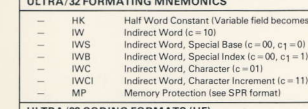
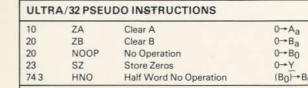
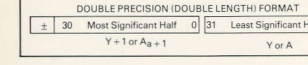
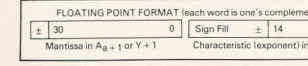
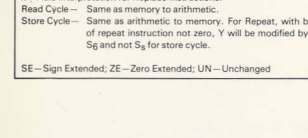
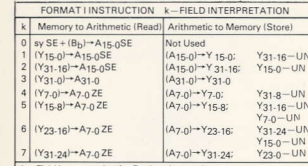
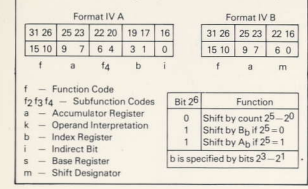
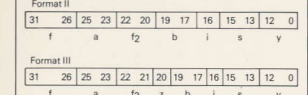
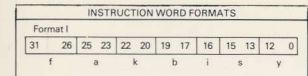


AN/UJK-7 COMPUTER
REPERTOIRE OF INSTRUCTIONS

CENTRAL PROCESSOR COMMANDS

Table of Central Processor Commands with columns: Code, Mnemonic, NAME, DESCRIPTION, F, CA, R, U, F, Time μS. Includes instructions like ILLEGAL, OR, AND, ADD, SUB, etc.

Table of Central Processor Commands with columns: Code, Mnemonic, NAME, DESCRIPTION, F, CA, R, U, F, Time μS. Includes instructions like ILLEGAL, BZ, BS, RA, RI, RAN, RD, M, D, BC, CXI, C, CL, CM, CG, JEP, JOP, DJZ, DNJZ, JP, JN, JZ, JNZ, LBJ, LBN, J, JL, JNF, JOF, JNE, JEQ, JGT, JGE, JLT, JLE, JNW, JW, RJ, RJC, RJSC, J, JSC, LCT, LCI, SCT, SCI, HSC, HSC, HLCI, HLC, HRZ, HDRZ, HRS, HDRS, HSF, HDSP, HCP, HDPC, ILLEGAL, HOR, HA, HAN, HXR, HND, ILLEGAL, HD, HRT, HLB, HCL, HCR, HCB, ILLEGAL, HM, HD, HRT, HLB, HCL, HCR, HCB, ILLEGAL, HSIM, HSTC, ILLEGAL, HPI, HALT, HWT, ILLEGAL.



CENTRAL PROCESSOR CONTROL MEMORY ADDRESS ASSIGNMENT

Table of Central Processor Control Memory Address Assignment with columns: Address, Use, Bits. Lists addresses for Accumulator (A) registers, Index (B) registers, Base (S) registers, Interrupt Mode, and ICW registers.

*Clock is lower order 16 bits
**Not Addressable in the Task Mode.
(Prievileged instruction only will occur)
Upper 16 bits used for index and arithmetic functions.
Lower three bits used only as base-register designation.

LBMP (05 4) CONSIDERATIONS
1) The LBMP instruction is privileged when bit 8 of the ASR = 0, but if bit 8 of the ASR = 1 and s#7 = a = 7)
2) All function codes except the 05 4 (LBMP) are privileged when bit 8 of the ASR = 1 and s#7 = 7 in the instruction.

ULTRA/32 CODING FORMATS (UF)
No. Variable Field, No. Variable Field, No. Variable Field, No. Variable Field, No. Variable Field, No. Variable Field

(An Asterisk (*) Preceding Y Indicates Indirect Addressing)
ULTRA/32 CODING FORMATS (UF)
No. Variable Field, No. Variable Field, No. Variable Field, No. Variable Field, No. Variable Field, No. Variable Field

SYMBOL DEFINITIONS
CMR - Control Memory Register
F - Format
CA - Character Addressable
R - Repeatable
DSW - Designator Storage Word
UF - Ultra Format
IA - Contents of A, bit n
CD - Compare Designator
Y - Addressed format by Y (B) + (S)
ICW - Initial Condition Word
Y - Operand (Y) (Whole word or partial word or Y, depending on k
- Logical product (AND)
- Logical sum (Inclusive OR)
- Logical difference (Exclusive OR)

I/O CONTROLLER COMMANDS

(All Unused Function Codes are Illegal)

Code	Mnemonic	NAME	DESCRIPTION	UF**	Time μ S
10	IB	Initiate Input Buffer on Cj	(y) = CMA* 0 + j; Activate Input	1	3.25
11	OB	Initiate Output Buffer on Cj	(y) = CMA* 20 + j; Activate Output	1	3.25
12	FB	Initiate External Function Buffer on Cj	(y) = CMA* 40 + j; Activate EF	1	3.25
13	XB	Initiate External Interrupt Buffer on Cj	(y) = CMA* 60 + j; Activate EI	1	3.25
14k=0	TIB†	Terminate Input Buffer on Cj	Terminate Input m = 0 Suppress	2	3.0
14k=1	TOT†	Terminate Output Buffer on Cj	Terminate Output m = 0 Queued Interrupt;	2	3.0
14k=2	TFT†	Terminate External Function Buffer on Cj	Terminate EF m = 1 Allow Queued	2	3.0
14k=3	TXB†	Terminate External Interrupt Buffer on Cj	Terminate EI Interrupt	2	3.0
15k=0	IMIR	Set Input Monitor Interrupt Request on Cj	Set Input Monitor Interrupt on Chan j	3	2.5
15k=1	OMIR	Set Output Monitor Interrupt Request on Cj	Set Output Monitor Interrupt on Chan j	3	2.5
15k=2	FMIR	Set EF Monitor Interrupt Request on Cj	Set EF Monitor Interrupt on Chan j	3	2.5
15k=3	XMIR	Set EI Monitor Interrupt Request on Cj	Set EI Monitor Interrupt on Chan j	3	2.5
16k=0	AIC	Set Input Chain Active on Cj	y = Command Address Pointer Field	4	2.5
16k=1	AOC†	Set Output Chain Active on Cj	(bits 55-38) of CMA* 20k + j;	4	2.5
16k=2	AFC	Set External Function Chain Active on Cj	Activate Chain	4	2.5
16k=3	AXC	Set External Interrupt Chain Active on Cj		4	2.5
17m=0	TBZ	Test Bit Zero	If (y)k = 0, SKIP; Else NI	7	4.0
17m=1	TBS	Test Bit Set	If (y)k ≠ 0, SKIP; Else NI	7	4.0
20	JIO	Jump to y	y = Command Address Pointer or CARH	6	2.5
22	LICM	Load IOC Control Memory	(y) = IOC Control Memory Address k j	5	3.25
23	ILTC	Load Real-Time Clock	(y) = Real Time Clock	6	4.0
24	SICM	Show IOC Control Memory	(IOC Control Memory)k j = y	5	2.75
25	IBS	Set Bit	1 = yk	5	3.25
26	IBZ	Clear Bit	0 = yk	5	3.25
27	ITSF	Test and Set Flag	1 = y31; If (y)31 was Originally Cleared, SKIP; Else NI	6	3.25

FORMATING MNEMONICS

—	BCW	Buffer Control Word	8	—
—	BCWE	Buffer Control Word ESI	9	—

**ULTRA FORMAT				
† Command Address Register	1—j, y, k, c, m	4—j, y, c	7—k j, y	(l = buffer length)
* Control Memory Address	2—j, c, m	5—k j, y, c	8—y, j, k	
	3—j, c	6—y, c	9—y, j, k	

k—DESIGNATOR DEFINITIONS

k=0	k=1	k=2	k=3
f=10, 11, 13	Suppress data	Pack Quarter word	Pack Half word
f=12	Force One Word (y) is EF	One Word Buffer (y) is EF	Multi Word Buffer
			Not Used

† The terminate buffer commands terminate only active buffers. They have no effect on active chains. Terminating an active buffer also terminates the chain since the buffer never completed normally. To terminate an active chain, it is recommended that a JIO instruction with no chaining be initiated on the channel & function to be terminated (y may be any valid address). However, attempts to terminate a chain on a channel and function with an active buffer will result in the CAP being overlaid but no change to the chain bit in IOCM. In this case, the buffer will complete normally and chaining will commence with the JIO instruction which then terminates the chain.

Note: Clearing the IOC enables all monitor interrupts to all CPU's (i.e., all bits set in all ILR's) and clears all requests.

IOC COMMAND WORD FORMAT

31	26	25	24	23	20	19	18	17	0
Function Code f	Partial Word Desig.	Channel (0-17)	Number	Pointer	Buffer	Chain Flag	Monitor Interrupt Flag	Operand Address y	Compare Bits

NORMAL BUFFER CONTROL WORD FORMAT

31	18	17	0
Final Address	Initial Address	Compare Bits	

IOC CONTROL MEMORY WORD FORMAT

55	38	37	36	35	34	33	32	31	18	17	0
Command Address Pointer	Partial Word Desig.	Byte Pointer	Final Pointer	Buffer	Chain Flag	Monitor Interrupt Flag	Current Address	Current Address	Current Address	Current Address	Current Address

ESI BUFFER CONTROL WORD FORMAT

31	29	28	18	17	0
Partial Word Desig.	Final Address	Compare Bits	Current Address	Current Address	Current Address

Partial Word Desig. Definitions

31	30	29	Quarter Word XX = 00 next byte 31-24
X	X	1	01 next byte 23-16
X	1	0	Half Word X = 0 next word 31-16
1	0	0	X = 1 next word 15- 0
1	0	0	Full Word
0	0	0	Suppress Data*

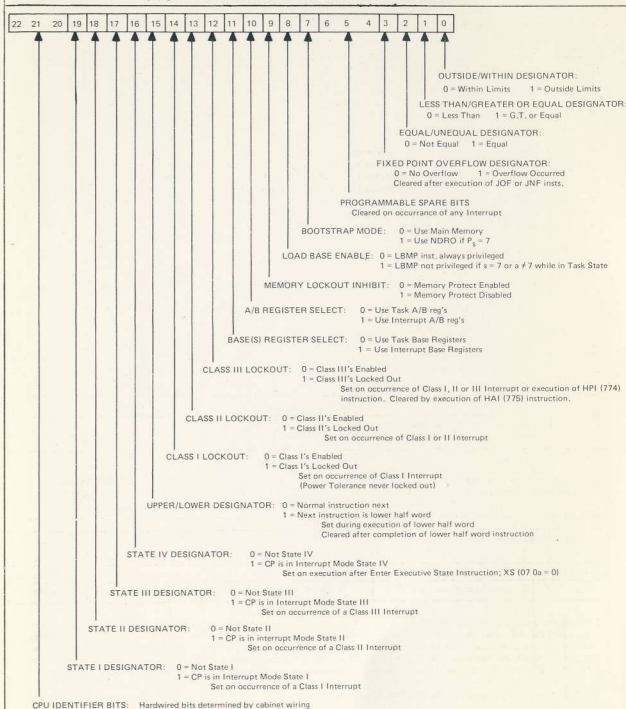
Maximum ESI Buffer is 2048 Words

* Suppress Data stores zeros at the specified address on input (ESI only)

IOC CONTROL MEMORY ASSIGNMENT

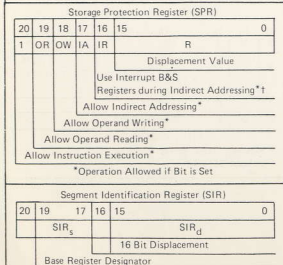
Address	Assignment
0-17	Input
20-37	Output
40-57	External Function
60-77	External Interrupt

ACTIVE STATUS REGISTER FORMAT



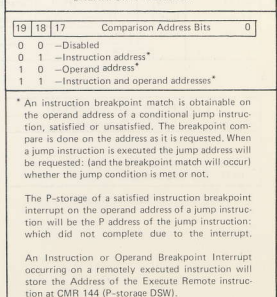
Note: The State bits (19-15) are mutually exclusive. Operation with multiple State bits set is "UNDEFINED."
The Task State is defined as bits 19-16 = 0
The Interrupt State is defined as any bit 19-16 ≠ 0
Bits 11-9 are normally cleared for Task and set for the Interrupt States. However, this is not a requirement.
The SCT, HSCT instructions store all 23 bits of the ASR. However, the LCT or HLCT load only bits 14-0.
To load all 23 bits of the ASR, an IR must be performed.

MEMORY PROTECTION REGISTERS



† For complete description of all possible uses, consult the equipment specification NAVSHIPS 0967-051-6291, also, see notes under repeat and indirect addressing tables.

BREAKPOINT REGISTER



PROGRAMMER NOTES

USE A PENCIL FOR ENTRIES AND CHANGES MAY BE MADE WITH AN ERASER.

IOC BUFFERED REQUEST PRIORITY

REQUEST PRIORITY	REQUEST TITLE	ACTION WHEN PROCESSED
Channel dependent	Buffer request (includes EI, EF, outputs and input)	Performs transfer based on buffer request priority first by channel (17 highest, 0 lowest) then as specified below.
1a	External interrupt request (occurs when an external device sets the external interrupt request line)	Performs a one word external interrupt word transfer using the control memory word at CMR address for channel.
1b	External function request (occurs when an external device sets the external function request line)	Performs a one word external function code word transfer using the control memory word at CMR address for channel.
1c	Output data request (occurs when an external device sets the output data request line)	Performs a one word output data word transfer using the control memory word at CMR address for channel.
1d	Input data request (occurs when an external device sets the input data request line)	Performs a one word input data word transfer using the control memory word at CMR address for channel.

IOC REQUEST (NONBUFFERED) PRIORITY

PRIORITY REQUEST	REQUEST TITLE	ACTION WHEN PROCESSED
1	Intercomputer Terminate Sequence	Performs the termination functions when an intercomputer channel terminates.
2	Clock Request	Decrement the IOC monitor clock by 1 and increment the real-time clock by 1.
3	Central Processor Instruction for IOC and Interrupt Status Code Requests.	Performs the function as commanded according to priority below.
3a	CP No. 0 Request*	
3b	CP No. 1 Request*	
3c	CP No. 2 Request*	
4	Central Processor Command Address Request	Performs the function as commanded according to priority below.
4a	CP No. 0 Request	* The numbers 1 & 2 are IOC port numbers and not necessarily the same as CPU I.D.
4b	CP No. 1 Request	
4c	CP No. 2 Request	
5	Chain Commands (Note 1) (channel associated)	Performs the function as commanded according to normal channel priority.

Note 1: For buffer terminations with the chain bit (IOCM 35) set, normal priority is bypassed and the next sequential command in that chain is executed.

IOC MAINTENANCE CONSOLE DISPLAY

REGISTER SELECT	CM ADDRESS SELECT/SELECT 2	I/O CONTROLLER DISPLAY (IOC must be in SEQ mode)	MON/ CHAIN
CMP	0-77	Bits 55-36 of IOCM (CAP) specified by CM ADDRESS SELECT	N.U.
CMU	0-77	Bits 37, 36 and 33-18 of IOCM specified by CM ADDRESS SELECT	bit 35 (chain)
CML	0-77	Bits 17-0 of IOCM specified by CM ADDRESS SELECT	bit 34 (monitor)
DIRU	N.U.	Bits 31-18 of DIR	N.U.
DIRL	N.U.	Bits 17-0 of DIR	N.U.
SEL 2	CAR + 0	(CAR 0) bits 17-0†	CAR ACT.
	CAR + 1	(CAR 1) bits 17-0†	CAR ACT.
	CAR + 2	(CAR 2) bits 17-0†	CAR ACT.
	ILR + 0	(ILR 0) channels 15-0†	N.U.
	ILR + 1	(ILR 1) channels 15-0†	N.U.
	ILR + 2	(ILR 2) channels 15-0†	N.U.
	CHAN + 0	Buffer actives by type on channels 3-0†	N.U.
	CHAN + 1	Buffer actives by type on channels 7-4†	N.U.
	CHAN + 2	Buffer actives by type on channels 10-13†	N.U.
	CHAN + 3	Buffer actives by type on channels 17-14†	N.U.
	CHAIN + 0	Chain actives by type on channels 3-0†	N.U.
	CHAIN + 1	Chain actives by type on channels 7-4†	N.U.
	CHAIN + 2	Chain actives by type on channels 13-10†	N.U.
	CHAIN + 3	Chain actives by type on channels 17-14†	N.U.
	60	(RTC) bits 17-0	CAR 0 ACTIVE
	61	(RTC) bits 31-18	CAR 1 ACTIVE
	62	(IOC MONITOR CLK) 15-0	N.U.

N.U. Not Used

† These displays are indicate only and are available in both RUN and SEQ mode.

‡ These displays are available in both RUN and SEQ mode.