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AN/UYK-7(V)

TECHNICAL SUMMARY HANDBOOK

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NAVSEA 0967-LP-024-5800

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AN/UYK-7(V) TECHNICAL SUMMARY HANDBOOK

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FOREWORD

The AN/UYK-7(V) Technical Summary Handbook (NAVSEA 0967-LP-024-5800) is a quick-reference document which contains information related to the operation of the AN/UYK-7(V) Computer and associated peripheral equipments.

This handbook contains the repertoire of instructions for both the Central Processor Unit (CPU) and the Input/Output Controller (IOC). Further, there is information on the Mode Selectors, Nondestructive Readout (NDRO) Memory, and peripheral equipment command/interrupt formats. In addition, this handbook also contains Chassis Maps, Line Replaceable Units (LRUs), and cable and interface connections.

For more detailed information about the data contained in this handbook, refer to the Maintenance Manual for Computer Set AN/UYK-7(V) SE610-AW-MMA-010, -020, -030, or -040.

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REPERTOIRE OF INSTRUCTIONS

Code	Mnemonic	NAME	DESCRIPTION	F	CA	R	UF	Time‡ μS
00	ILLEGAL							
01 0	OR	Inclusive OR (Selective Set A)	$(Y) \oplus (A_a) \rightarrow A_a$	II	Y	Y	2	1.5
01 1	SC	Selective Clear A	$(A_a) \odot (Y)' \rightarrow A_a$	II	Y	Y	2	1.5
01 2	MS	Selective Substitute	$(Y)_n \rightarrow (A_a + 1)_n$ for all $(A_a)_n = 1$; $(A_a)_i = (A_a)_f$	II	Y	Y	2	1.5
01 3	XOR	Exclusive OR (Sel. Comp. A)	$(Y) \bar{\oplus} (A_a) \rightarrow A_a$; $(A_a)_n' \rightarrow (A_a)$ for $(Y)_n = 1$	II	Y	Y	2	1.5
01 4	ALP	Add Logical Product	$(A_a + 1) + (Y) \odot (A_a) \rightarrow A_a + 1$; $(A_a)_i = (A_a)_f$	II	Y	Y	2	1.5
01 5	LLP	Load Logical Product	$(Y) \odot (A_a) \rightarrow A_a$	II	Y	Y	2	1.5
01 6	NLP	Subtract Logical Product	$(A_a + 1) - (Y) \odot (A_a) \rightarrow A_a + 1$; $(A_a)_i = (A_a)_f$	II	Y	Y	2	1.5
01 7	LLPN	Load Logical Product Next	$(Y) \odot (A_a) \rightarrow A_a + 1$; $(A_a)_i = (A_a)_f$	II	Y	Y	2	1.5
02 0	CNT	Count Ones	No. of Bits Set in $(Y) \rightarrow A_a$	II	Y	Y	2	7.5†
02 1	ILLEGAL							
02 2	XR	Execute Remote	$(Y) \rightarrow U$. Execute $(Y)_u$ only of two half words.	II	N	N	8	1.5
02 3	XRL	Execute Remote Lower	$(Y)_L \rightarrow U$	II	N	N	8	1.5
02 4	SLP	Store Logical Product	$(A_a + 1) \odot (A_a) \rightarrow Y$; $(A_a)_i = (A_a)_f$; $(A_a + 1)_i = (A_a + 1)_f$	II	Y	Y	2	1.5
02 5	SSUM	Store Sum	$(A_a) + (A_a + 1) \rightarrow A_a + 1 \& Y$; $(A_a)_i = (A_a)_f$	II	Y	Y	2	2.0
02 6	SDIF	Store Difference	$(A_a + 1) - (A_a) \rightarrow A_a + 1 \& Y$; $(A_a)_i = (A_a)_f$	II	Y	Y	2	2.0
02 7††	DS	Double Store A	$(A_a + 1, A_a) \rightarrow Y + 1, Y$	II	N	N	2	3.0
03 0	ROR	Replace Inclusive OR	$(Y) \oplus (A_a) \rightarrow A_a \& Y$	II	Y	Y	2	2.5

03 1	RSC	Replace Selective Clear	$(A_a) \odot (Y)' \rightarrow A_a \& Y$	II	Y	Y	2	2.5
03 2	RMS	Replace Selective Substitute	$(Y)_n \rightarrow (A_a + 1)_n$ for all $(A_a)_n = 1$; Then $(A_a + 1) \rightarrow Y$; $(A_a)_i = (A_a)_f$	II	Y	Y	2	2.5
03 3	RXOR	Replace Exclusive OR	$(Y) \bar{\oplus} (A_a) \rightarrow A_a \& Y$; $(A_a)_n' \rightarrow A_a \& Y$ for $Y_n = 1$	II	N	Y	2	2.5
03 4	RALP	Replace A + Logical Product	$(A_a + 1) + (Y) \odot (A_a) \rightarrow A_a + 1 \& Y$; $(A_a)_i = (A_a)_f$	II	Y	Y	2	2.5
03 5	RLP	Replace Logical Product	$(Y) \odot (A_a) \rightarrow Y \& A_a + 1$; $(A_a)_i = (A_a)_f$	II	Y	Y	2	2.5
03 6	RNLP	Replace A − Logical Product	$(A_a + 1) - (Y) \odot (A_a) \rightarrow A_a + 1 \& Y$; $(A_a)_i = (A_a)_f$	II	Y	Y	2	2.5
03 7	TSF	Test and Set Flag	If $(Y)_{31} = 0$, CD Set EQUAL. $1 \rightarrow Y_{31}$ If $(Y)_{31} = 1$, CD Set UNEQUAL. This instruction cannot use indirect addressing.	II	N	Y	8	2.5
04 X	ILLEGAL							
05 0††	DL	Double Load A	$(Y + 1, Y) \rightarrow A_a + 1, A_a$	II	N	N	2	3.0
05 1††	DA	Double Add A	$(A_a + 1, A_a) + (Y + 1, Y) \rightarrow A_a + 1, A_a$	II	N	N	2	3.0
05 2††	DAN	Double Subtract A	$(A_a + 1, A_a) - (Y + 1, Y) \rightarrow A_a + 1, A_a$	II	N	N	2	3.0
05 3††	DC	Double Compare	Compare $(A_a + 1, A_a)$ to $(Y + 1, Y)$, Set CD	II	N	N	2	3.0
05 4	LBMP	Load Base and Memory Protection	$(Y)_{17\text{-}0} \rightarrow S_a$; $(Y + 1)_{20\text{-}0} \rightarrow SPR_a$; $Y \rightarrow SIR_a$ Privileged if: ASR bit 8 = 0, s≠7 or a = 7. Illegal if $y + (B_b)$ = odd.	II	N	N	2	5.75
05 5	ILLEGAL							
05 6	ILLEGAL							
05 7	ILLEGAL							
06 0††	FA	Floating-point Add	Shift $(A_a + 1)$ or $(Y + 1)$ Right such that $(A_a) = (Y)$ $(A_a + 1) + (Y + 1) \rightarrow A_a + 1$; Normalize	II	N	N	2	6.25†

REPERTOIRE OF INSTRUCTIONS (continued)

Code	Mnemonic	NAME	DESCRIPTION	F	CA	R	UF	Time‡ μS
06 1††	FAN	Floating-point Subtract	Shift (A_a+1) or $(Y+1)$ Right such that $(A_a)=(Y)$ $(A_a+1)-(Y+1)\rightarrow A_a+1$; Normalize	II	N	N	2	6.25†
06 2††	FM	Floating-point Multiply	$(A_a)+(Y)\rightarrow(A_a)$ $(A_a+1)\bullet(Y+1)\rightarrow A_a+1$; Normalize	II	N	N	2	10.0†
06 3††	FD	Floating-point Divide	$(A_a)-(Y)\rightarrow(A_a)$ $(A_a+1)\div(Y+1)\rightarrow A_a+1$; Normalize	II	N	N	2	17.0†
06 4††	FAR	Floating-point Add with Round	Same as FA with (A_a+1) rounded	II	N	N	2	6.25†
06 5††	FANR	Floating-point Subtract w/Rd.	Same as FAN with (A_a+1) rounded	II	N	N	2	6.25†
06 6††	FMR	Floating-point Multiply w/Rd.	Same as FM with (A_a+1) rounded	II	N	N	2	10.0†
06 7††	FDR	Floating-point Divide w/Rd.	Same as FD with (A_a+1) rounded	II	N	N	2	17.0
07 0 a=0	XS	Enter Executive State	$sy+(B_b)\rightarrow$CMR 156; Enter class IV(Executive)	II	N	N	11	4.0
07 0* a=1	IPI	Interprocessor Interrupt	Send Class II interrupt to processors n (0-7) IF bit n of $sy+(B_b)=1$. Prevent self-interrupt if $sy+(B_b)$ bit 15 = 1.	II	N	N	11	4.0
07 1**	AEI	Allow Enable Interrupt	Allow Monitor interrupts from IOC a on Channels n; IF bit n of $sy+(B_b)=1$: Bit 25 is ignored	II	N	N	6	2.0
07 2**	PEI	Prevent Enable Interrupt	Prevent Monitor interrupts from IOC a on Channels n; IF bit n of $sy+(B_b)=1$: Bit 25 is ignored	II	N	N	6	2.0

07 3**	LIM	Load IOC Monitor Clock	$sy+(B_b)\rightarrow$IOC a MON CLK	II	N	N	6	3.0
07 4**	IO	Initiate I/O	Initiate IOC a at address Y	II	N	N	2	3.5
07 5*	IR	Interrupt Return	Return from highest State Specified by ASR bits 19-16.	II	N	N	9	3.0
07 6	RP	Repeat	Repeat N.I.B_7 Times; sy sign extended of Repeat added to B_b of N.I. after each cycle. See Repeat Conditions Illegal if in N.I. i = 1 and c = 00.	II	N	N	6	1.5
07 7	ILLEGAL							
10	LA	Load A	$\underline{Y}\rightarrow A_a$	I	Y	Y	1	1.5
11††	LXB	Load A and Index B	$\underline{Y}\rightarrow A_a$; $(B_b+1\rightarrow B_b$. Illegal if i = 1 and cc = 00.	I	Y	N	1	1.5
12	LDIF	Load Difference	$\underline{Y}-(A_a)\rightarrow A_a+1$; $(A_a)_i=(A_a)_f$	I	Y	Y	1	1.5
13	ANA	Subtract A	$(A_a)-\underline{Y}\rightarrow A_a$	I	Y	Y	1	1.5
14	AA	Add A	$(A_a)+\underline{Y}\rightarrow A_a$	I	Y	Y	1	1.5
15	LSUM	Load Sum	$(A_a)+\underline{Y}\rightarrow A_a+1$; $(A_a)_i=(A_a)_f$	I	Y	Y	1	1.5
16	LNA	Load Negative	$\underline{Y}'\rightarrow A_a$	I	Y	Y	1	1.5
17	LM	Load Magnitude	$\lvert\underline{Y}\rvert\rightarrow A_a$	I	Y	Y	1	1.5
20	LB	Load B	$\underline{Y}\rightarrow B_a$	I	Y	Y	1	2.0
21	AB	Add B	$(B_a)+\underline{Y}\rightarrow B_a$; B_a zero extended	I	Y	Y	1	2.0
22	ANB	Subtract B	$(B_a)-\underline{Y}\rightarrow B_a$; B_a zero extended	I	Y	Y	1	2.0
23	SB	Store B	$(B_a)\rightarrow\underline{Y}$	I	Y	Y	1	1.5
24	SA	Store A	$(A_a)\rightarrow\underline{Y}$	I	Y	Y	1	1.5
25††	SXB	Store A and Index B	$(A_a)\rightarrow\underline{Y}$; $(B_b)+1\rightarrow B_b$. Illegal if i = 1 and cc = 00.	I	Y	N	1	1.5

REPERTOIRE OF INSTRUCTIONS (continued)

Code	Mnemonic	NAME	DESCRIPTION	F	CA	R	UF	Time‡ μS
26	SNA	Store Negative	$(A_a)' \rightarrow \underline{Y}$	I	N	Y	1	1.5
27	SM	Store Magnitude	$\lvert(A_a)\rvert \rightarrow \underline{Y}$	I	N	Y	1	1.5
30	ILLEGAL							
31	ILLEGAL							
32	BZ	Clear Bit	$0 \rightarrow Y_{ak}$	I	N	Y	3	2.5
33	BS	Set Bit	$1 \rightarrow Y_{ak}$	I	N	Y	3	2.5
34	RA	Replace Add	$(A_a) + \underline{Y} \rightarrow A_{a+1}$ & $\underline{Y}$; $(A_a)_i = (A_a)_f$	I	Y	Y	1	2.5
35	RI	Replace Increment	$\underline{Y} + 1 \rightarrow A_a$ & $\underline{Y}$	I	Y	Y	1	2.5
36	RAN	Replace Subtract	$\underline{Y} - (A_a) \rightarrow A_{a+1}$ & $\underline{Y}$; $(A_a)_i = (A_a)_t$	I	Y	Y	1	2.5
37	RD	Replace Decrement	$\underline{Y} - 1 \rightarrow A_a$ & $\underline{Y}$	I	Y	Y	1	2.5
40	M	Multiply A	$(A_a) \bullet \underline{Y} \rightarrow A_{a+1}, A_a$	I	Y	Y	1	7.5†
41	D	Divide A	$(A_{a+1}, A_a) \div \underline{Y} \rightarrow A_a$; remainder $\rightarrow A_{a+1}$	I	Y	Y	1	14.5†
42	BC	Compare Bit to Zero	If $(Y)_{ak} = 0$, CD Set EQUAL If $(Y)_{ak} = 1$, CD Set UNEQUAL Bit 25 is ignored	I	N	Y	3	1.5
43	CXI	Compare Index Increment	If $(B_a) \geq \underline{Y}$, CD Set OUTSIDE, $0 \rightarrow B_a$ If $(B_a) < \underline{Y}$, CD Set WITHIN, $(B_a) + 1 \rightarrow B_a$	I	Y	N	1	2.0
44	C	Compare	Compare (A_a) to $\underline{Y}$, Set the CD	I	Y	Y	1	1.5
45	CL	Compare Limits	If $(A_{a+1}) > \underline{Y} \geq (A_a)$, Set CD WITHIN	I	Y	Y	1	1.5
46	CM	Compare Masked	Compare (A_{a+1}) to $(A_a) \odot \underline{Y}$, Set the CD	I	Y	Y	1	1.5

47	CG	Compare Gated	Compare $\lvert\underline{Y} - (A_a)\rvert$ to (A_{a+1}), Set the CD	I	Y	Y	1	1.5
50 0	JEP	Jump on Even Parity	If $(A_{a+1}) \odot (A_a)$ is Even Parity, jump to Y	III	N	N	1	2.0
50 1	JOP	Jump on Odd Parity	If $(A_{a+1}) \odot (A_a)$ is Odd Parity, jump to Y	III	N	N	1	2.0
50 2	DJZ	Jump Double Precision Zero	If $(A_{a+1}, A_a) = 0$, jump to Y	III	N	N	1	2.0
50 3	DJNZ	Jump Double Precision Not Zero	If $(A_{a+1}, A_a) \neq 0$, jump to Y	III	N	N	1	2.0
51 0	JP	Jump A Positive	If $(A_a) \geq 0$, jump to Y	III	N	N	1	1.5
51 1	JN	Jump A Negative	If $(A_a) < 0$, jump to Y	III	N	N	1	1.5
51 2	JZ	Jump A Zero	If $(A_a) = 0$, jump to Y	III	N	N	1	1.5
51 3	JNZ	Jump A Not Zero	If $(A_a) \neq 0$, jump to Y	III	N	N	1	1.5
52 0	LBJ	Load B and Jump	$(P) + 1 \rightarrow B_a$, jump to Y	III	N	N	1	1.8
52 1	JBNZ	Index Jump B	If $(B_a) \neq 0$, then $(B_a) - 1 \rightarrow B_a$, jump to Y	III	N	N	1	1.8
52 2	JS	Jump sy + B	$[sy + (B_b)_{15-0}]_{ZE}$ and $(B_b)_{19-17} \rightarrow P_{19-17}$	III	N	N	13	1.5
52 3	JL	Unconditional Jump Lower	Jump to the Lower of Y	III	N	N	12	1.5
53 0 a = 0	JNF	Jump on No Overflow	If OD is not Set, Jump to Y; Clear OD	III	N	N	12	1.5
53 0 a = 1	JOF	Jump on Overflow	If OD is Set, jump to Y; Clear OD	III	N	N	12	1.5
53 1 a = 0	JNE	Jump on Not Equal	If CD ≠, jump to Y	III	N	N	12	1.5
53 1 a = 1	JE	Jump on Equal	If CD =, jump to Y	III	N	N	12	1.5
53 1 a = 2	JG	Jump on Greater Than	If CD >, jump to Y	III	N	N	12	1.5
53 1 a = 3	JGE	Jump on Greater Than or Equal	If CD ≥, jump to Y	III	N	N	12	1.5
53 1 a = 4	JLT	Jump on Less Than	If CD <, jump to Y	III	N	N	12	1.5
53 1 a = 5	JLE	Jump on Less Than or Equal	If CD ≤, jump to Y	III	N	N	12	1.5
53 1 a = 6	JNW	Jump Outside Limits	If CD Outside Limits, jump to Y	III	N	N	12	1.5
53 1 a = 7	JW	Jump Within Limits	If CD Within Limits, jump to Y	III	N	N	12	1.5

REPERTOIRE OF INSTRUCTIONS (continued)

Code	Mnemonic	NAME	DESCRIPTION	F	CA	R	UF	Time‡ μS
53 2	RJ	Return Jump a = o	(P)+ 1→Y, jump to Y + 1	III	N	N	12	3.0
53 2	RJC	Return Jump a = 1, 2, 3	If switch a is Set, (P) + 1→Y, jump to Y + 1; otherwise N.I.	III	N	N	1	3.0
53 2*	RJSC	Return Jump a = 4, 5, 6, 7	If switch a is Set, Stop; (P)+ 1→Y, jump to Y + 1 at restart	III	N	N	1	3.75
53 3	J	Manual Jump a = o	Jump to Y	III	N	N	12	1.5
53 3	JC	Manual Jump a = 1, 2, 3	If switch a is Set, jump to Y; otherwise N.I.	III	N	N	1	1.5
53 3*	JSC	Manual Jump a = 4, 5, 6, 7	If switch a is Set, Stop; Jump to Y at restart	III	N	N	1	2.25
54↙	LCT	Load CMR Task	$(Y)\rightarrow CMR_{ak}$	I	N	Y	3	1.5
55*	LCI	Load CMR Interrupt	$(Y)\rightarrow CMR_{ak+100}$	I	N	Y	3	1.5
56↙	SCT	Store CMR Task	$(CMR_{ak})\rightarrow Y$	I	N	Y	3	1.5
57*	SCI	Store CMR Interrupt	$(CMR_{ak+100})\rightarrow Y$	I	N	Y	3	1.5
60↙ i = 0	HSCT	Store CMR in A	$(CMR_{af4})\rightarrow A_b$	IV A	N	N	4	1.75
60* i = 1	HSCI	Store CMR in A	$(CMR_{af+100})\rightarrow A_b$	IV A	N	N	4	1.75
61↙ i = 0	HLCT	Load CMR from A	$(A_b)\rightarrow CMR_{af4}$	IV A	N	N	4	1.7
61* i = 1	HLCI	Load CMR from A	$(A_b)\rightarrow CMR_{af4+100}$	IV A	N	N	4	1.75
62	HLC	Shift Left Circularly	(A_a) Left Shifted End Around→A_a	IV B	N	N	10	1.75
63	HDLC	Shift Left Circularly Double	(A_{a+1}, A_a) Left Shifted End Around→A_{a+1}, A_a	IV B	N	N	10	1.75
64	HRZ	Shift Right Fill Zeros	(A_a) Right Shifted, Zero Fill→A_a	IV B	N	N	10	1.75
65	HDRZ	Shift Right Double, Fill Zeros	(A_{a+1}, A_a) Right Shifted, Zero Fill→A_{a+1}, A_a	IV B	N	N	10	1.75

load/store only bits 15–0 of B

66	HRS	Shift Right Fill Sign	(A_a) Right Shifted, Sign Fill→A_a	IV B	N	N	10	1.75
67	HDRS	Shift Right Double, Fill Sign	(A_{a+1}, A_a) Right Shifted Sign Fill→A_{a+1}, A_a	IV B	N	N	10	1.75
70 0	HSF	Scale Factor	Normalize (A_a) Shift Count→A_b	IV A	N	N	5	2.25
70 1	HDSF	Double Scale Factor	Normalize (A_{a+1}, A_a) Shift Count→A_b	IV A	N	N	5	2.25
70 2	HCP	Complement A	$(A_a)'\rightarrow A_a$	IV A	N	N	7	1.1
70 3	HDCP	Double Complement A	$(A_{a+1}, A_a)'\rightarrow A_{a+1}, A_a$	IV A	N	N	7	1.1
70 4	ILLEGAL							
70 5	ILLEGAL							
70 6	ILLEGAL							
70 7	ILLEGAL							
71 0	HOR	Logical Sum	$(A_a) \oplus (A_b)\rightarrow A_a$; $(A_b)_i = (A_b)_f$ if $a \neq b$	IV A	N	N	5	1.0
71 1	HA	Sum	$(A_a) + (A_b)\rightarrow A_a$; $(A_b)_i = (A_b)_f$ if $a \neq b$	IV A	N	N	5	1.0
71 2	HAN	Difference	$(A_a) - (A_b)\rightarrow A_a$; $(A_b)_i = (A_b)_f$ if $a \neq b$	IV A	N	N	5	1.0
71 3	HXOR	Logical Difference	$(A_a) \overline{\oplus} (A_b)\rightarrow A_a$; $(A_b)_i = (A_b)_f$ if $a \neq b$	IV A	N	N	5	1.0
71 5	HAND	AND	$(A_a) \odot (A_b)\rightarrow A_a$; $(A_b)_i = (A_b)_f$ if $a \neq b$	IV A	N	N	5	1.0
71 6	ILLEGAL							
71 7	ILLEGAL							
72 X	ILLEGAL							
73 X	ILLEGAL							
74 0	HM	Multiply Register	$(A_a) \bullet (A_b)\rightarrow A_{a+1}, A_a$	IV A	N	N	5	7.75†
74 1	HD	Divide Register	$(A_{a+1}, A_a) \div (A_b)\rightarrow A_a$; Remainder→$A_{a+1}$	IV A	N	N	5	15.0†
74 2	HRT	Square Root	$\sqrt{(A_{a+1}, A_a)}\rightarrow A_b$; Residue→$A_{b+1}$	IV A	N	N	5	15.0†
74 3	HLB	Load B_a with B_b	$(B_b)\rightarrow B_a$	IV A	N	N	5	1.75
74 4	HC	Compare, Register	Compare (A_a) to (A_b), Set CD	IV A	N	N	5	1.1

REPERTOIRE OF INSTRUCTIONS (continued)

Code	Mnemonic	NAME	DESCRIPTION	F	CA	R	UF	Time‡ μS
74 5	HCL	Compare Limits, Register	If $(A_a+1) > (A_b) \geq (A_a)$, Set CD WITHIN	IV	A	N	N 5	1.75
74 6	HCM	Compare Masked, Register	Compare $(A_a+1) \odot (A_a)$ to (A_b), Set the CD	IV	A	N	N 5	1.1
74 7	HCB	Compare B_b with B_a	Compare (B_b) to (B_a), Set the CD	IV	A	N	N 5	2.0
75 X	ILLEGAL							
76 X	ILLEGAL							
77 0**	HSIM	Store IOC Monitor Clock in A	$(IOC_a$ MON CLK$)\rightarrow A_b$	IV	A	N	N 5	3.0
77 1	HSTC	Store Real-Time Clock in A	$(IOC_a$ RTC$)\rightarrow A_b$	IV	A	N	N 5	3.5
77 2	ILLEGAL							
77 3	ILLEGAL							
77 4*	HPI	Prevent Class III Interrupts	Set Class III Interrupt Lockout in the ASR	IV	A	N	N 9	2.25
77 5*	HAI	Allow Class III Interrupts	Clear Class III Interrupt Lockout in the ASR	IV	A	N	N 9	2.25
77 6*i = 0	HALT	Stop Processor	Stop CPU (4-Stop); Continue at Restart	IV	A	N	N 9	2.25
77 6*i = 1	HWFI	Wait for Interrupt	Cease Memory References until Interrupted	IV	A	N	N 9	2.25
77 7	ILLEGAL							

*Privileged **CPU→IOC Instr. — Privileged ⌐ Privileged when ak = 2X, 6X, or 7X or Repeated.
†Execution time independent of overlap operation ††Privileged if i = 1 & $(SPR)_s$ bit 16 = 1.
‡Times shown assume 1.5μs memory with operands not in same bank as instructions (overlapped).

ULTRA/32 PSEUDO INSTRUCTIONS				F	CA	R	UF	Time ‡ μS
10	ZA	Clear A	$0\rightarrow A_a$	I	N	Y	7	1.5
20	ZB	Clear B	$0\rightarrow B_a$	I	N	Y	7	2.0
20	NOOP	No Operation	$0\rightarrow B_0$	I	N	Y	9	2.0
23	SZ	Store Zeros	$0\rightarrow \underline{Y}$	I	Y	Y	12	1.5
74 3	HNO	Half Word No Operation	$(B_0)\rightarrow B_0$	IV	A	N	N 9	1.75

ULTRA/32 FORMATTING MNEMONICS							
—	HK	Half Word Constant (Variable field becomes next halfword)	—	—	—	16	—
—	IW	Indirect Word (c = 10)	—	—	—	8	—
—	IWS	Indirect Word, Special Base (c = 00, c_1 = 0)	—	—	—	11	—
—	IWB	Indirect Word, Special Index (c = 00, c_1 = 1)	—	—	—	11	—
—	IWC	Indirect Word, Character (c = 01)	—	—	—	14	—
—	IWCI	Indirect Word, Character Increment (c = 11)	—	—	—	14	—
—	MP	Memory Protection (see SPR format)	—	—	—	15	—

ULTRA/32 CODING FORMATS (UF)

(An Asterisk (*) Preceding y Indicates Indirect Addressing)

No.	Variable Field	No.	Variable Field	No.	Variable Field	No.	Variable Field	No.	Variable Field	No.	Variable Field
1	a, y, k, b, s	4	af4, b	7	a	10	a, m (shift by m)	11	sy, b	14	y, w, p, b, s
2	a, y, b, s	5	a, b	8	y, b, s		a, b, 1 (shift by B_b)	12	y, k, b, s	15	r, i, or, ow, ia, ir
3	ak, y, b, s	6	a, sy, b	9	None		a, b, 2 (shift by A_b)	13	sy, k, b	16	e

INSTRUCTION WORD FORMATS

Format I

31 26	25 23	22 20	19 17	16	15 13	12 0
f	a	k	b	i	s	y

Format II

31 26	25 23	22 20	19 17	16	15 13	12 0
f	a	f_2	b	i	s	y

Format III

31 26	25 23	22 21	20	19 17	16	15 13	12 0
f	a	f_3	z	b	i	s	y

Format IV A

31 26	25 23	22 20	19 17	16
15 10	9 7	6 4	3 1	0
f	a	f_4	b	i

Format IV B

31 26	25 23	22 16
15 10	9 7	6 0
f	a	m

f – Function Code
f_2 f_3 f_4 – Subfunction Codes
a – Accumulator Register
k – Operand Interpretation
b – Index Register
i – Indirect Bit
s – Base Register
m – Shift Designator
z – Not Used (must be zero)

Bit 2^6	Function
0	Shift by count 2^5-2^0
1	Shift by B_b if $2^5=0$
1	Shift by A_b if $2^5=1$

b is specified by bits 2^3-2^1

FORMAT I INSTRUCTION k-FIELD INTERPRETATION

k	Memory to Arithmetic (Read)	Arithmetic to Memory (Store)	
0	sy SE + $(B_b)\rightarrow A_{15-0}$SE	Not Used	
1	$(Y_{15-0})\rightarrow A_{15-0}$SE	$(A_{15-0})\rightarrow Y_{15-0}$;	Y_{31-16} – UN
2	$(Y_{31-16})\rightarrow A_{15-0}$SE	$(A_{15-0})\rightarrow Y_{31-16}$;	Y_{15-0} – UN
3	$(Y_{31-0})\rightarrow A_{31-0}$	$(A_{31-0})\rightarrow Y_{31-0}$	
4	$(Y_{7-0})\rightarrow A_{7-0}$ ZE	$(A_{7-0})\rightarrow Y_{7-0}$;	Y_{31-8} – UN
5	$(Y_{15-8})\rightarrow A_{7-0}$ ZE	$(A_{7-0})\rightarrow Y_{15-8}$;	Y_{31-16} – UN Y_{7-0} – UN
6	$(Y_{23-16})\rightarrow A_{7-0}$ ZE	$(A_{7-0})\rightarrow Y_{23-16}$;	Y_{31-24} – UN Y_{15-0} – UN
7	$(Y_{31-24})\rightarrow A_{7-0}$ ZE	$(A_{7-0})\rightarrow Y_{31-24}$;	Y_{23-0} – UN

k – Field Interpretation for Replace Instructions:
Read Cycle – Same as memory to arithmetic.
Store Cycle – Same as arithmetic to memory. For Repeat, with b of repeat instruction not zero, Y will be modified by S_6 and not S_S for store cycle.

SE – Sign Extended; ZE – Zero Extended; UN – Unchanged

SYMBOL DEFINITIONS

CMR – Control Memory Register
F – Format
CA – Character Addressable
R – Repeatable
DSW – Designator Storage Word
UF – Ultra Format
$(A)_n$ – Contents of A, bit n
CD – Compare Designator
Y – Address formed by y + (B_b) + (S_S)
ICW – Initial Condition Word
$\underline{Y}$ – Operand (Y) (Whole word or partial word) or Y, depending on k
$\odot$ – Logical product (AND)
$\oplus$ – Logical sum (Inclusive OR)
$\overline{\oplus}$ – Logical difference (Exclusive OR)

CENTRAL PROCESSOR CONTROL MEMORY ADDRESS ASSIGNMENT

Task Mode		
Address	Use	Bits
0-7	Accumulator (A) registers 0-7	32
10	Unassigned	19
11-17	Index (B) registers 1-7	19†
20-27	Base (S) registers 0-7**	18
30-57	Unassigned (not usable)	—
6x	Breakpoint register**	20
7x	Active status register**	23

Interrupt Mode		
Address	Use	Bits
100-107	Accumulator (A) registers 0-7	32
110	CP monitor clock register	19*
111-117	Index (B) registers 1-7	19†
120-127	Base (S) registers 0-7	18
130-137	Unassigned (not usable)	—
140	ICW—Class I	20
141	DSW—Class I ASR storage	20

142	DSW—Class I interrupt status code	20
143	DSW—Class I P—storage	20
144	ICW—Class II	20
145	DSW—Class II ASR storage	20
146	DSW—Class II interrupt status code	20
147	DSW—Class II P—storage	20
150	ICW—Class III	20
151	DSW—Class III ASR storage	20
152	DSW—Class III interrupt status code	20
153	DSW—Class III P—storage	20
154	ICW—Class IV	20
155	DSW—Class IV ASR storage	20
156	DSW—Class IV interrupt status code	20
157	DSW—Class IV P—storage	20
160-167	Storage Protection Registers (SPR) 0-7	21
170-177	Segment Identification Registers (SIR) 0-7	21

*Clock is low order 16 bits
**Not Addressable in the Task Mode.
(Privileged instruction error will occur)
†Lower 16 bits used for index and arithmetic functions.
Upper three bits used **only** as a base-register designation.

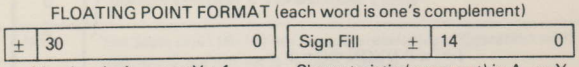
LBMP (05 4) CONSIDERATIONS

1) The LBMP instruction is privileged when bit 8 of the ASR = 0, or if bit 8 of the ASR = 1 and [s ≠ 7 or a = 7)

2) All function codes except the 05 4 (LBMP) are privileged when bit 8 of the ASR = 1 and s = 7 in the instruction.

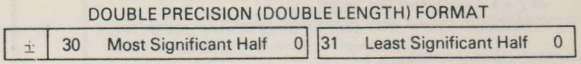
FLOATING POINT FORMATS

FLOATING POINT FORMAT (each word is one's complement)



Mantissa in $A_a + 1$ or Y + 1 — Characteristic (exponent) in A_a or Y

DOUBLE PRECISION (DOUBLE LENGTH) FORMAT

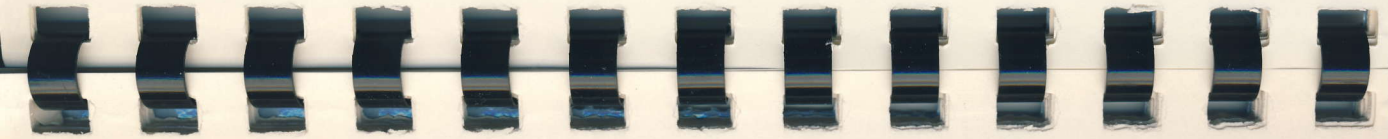


Y + 1 or $A_a + 1$ — Y or A

ACTIVE STATUS REGISTER FORMAT

BIT	DESCRIPTION
22 21 20	CPU IDENTIFIER BITS: Hardwired bits determined by cabinet wiring
19	STATE I DESIGNATOR: 0 = Not State I 1 = CP is in Interrupt Mode State I Set on occurrence of a Class I Interrupt
18	STATE II DESIGNATOR: 0 = Not State II 1 = CP is in interrupt Mode State II Set on occurrence of a Class II Interrupt
17	STATE III DESIGNATOR: 0 = Not State III 1 = CP is in Interrupt Mode State III Set on occurrence of a Class III Interrupt
16	STATE IV DESIGNATOR: 0 = Not State IV 1 = CP is in Interrupt Mode State IV Set on execution after Enter Executive State Instruction; XS (07 0a = 0)

BIT	DESCRIPTION
11	BASE(S) REGISTER SELECT: 0 = Use Task Base Registers 1 = Use Interrupt Base Registers
10	A/B REGISTER SELECT: 0 = Use Task A/B reg's 1 = Use Interrupt A/B reg's
9	MEMORY LOCKOUT INHIBIT: 0 = Memory Protect Enabled 1 = Memory Protect Disabled
8	LOAD BASE ENABLE: 0 = LBMP inst. always privileged 1 = LBMP not privileged if s = 7 or a ≠ 7 while in Task State
7	BOOTSTRAP MODE: 0 = Use Main Memory 1 = Use NDRO if P_s = 7
6 5 4	PROGRAMMABLE SPARE BITS Cleared on occurence of any Interrupt
3	FIXED POINT OVERFLOW DESIGNATOR: 0 = No Overflow 1 = Overflow Occurred Cleared after execution of JOF or JNF insts.



BIT	DESCRIPTION
15	UPPER/LOWER DESIGNATOR: 0 = Normal instruction next 1 = Next instruction is lower half word Set during execution of lower half word Cleared after completion of lower half word instruction
14	CLASS I LOCKOUT: 0 = Class I's Enabled 1 = Class I's Locked Out Set on occurrence of Class I Interrupt (Power Tolerance never locked out)
13	CLASS II LOCKOUT: 0 = Class II's Enabled 1 = Class II's Locked Out Set on occurrence of Class I or II Interrupt
12	CLASS III LOCKOUT: 0 = Class III's Enabled 1 = Class III's Locked Out Set on occurrence of Class I, II or III Interrupt or execution of HPI (774) instruction. Cleared by execution of HAI (775) instruction.

BIT	DESCRIPTION
2	EQUAL/UNEQUAL DESIGNATOR: 0 = Not Equal 1 = Equal
1	LESS THAN/GREATER OR EQUAL DESIGNATOR: 0 = Less Than 1 = G.T. or Equal
0	OUTSIDE/WITHIN DESIGNATOR: 0 = Within Limits 1 = Outside Limits

Note:

The State bits (19-16) are mutually exclusive. Operation with multiple State bits set is "UNDEFINED."

The Task State is defined as bits 19-16 = 0

The Interrupt State is defined as any bit 19--16 ≠ 0.

Bits 11-9 are normally cleared for Task and set for the Interrupt States. However, this is not a requirement.

The SCT, HSCT instructions store all 23 bits of the ASR. However, the LCT or HLCT load only bits 14-0. To load all 23 bits of the ASR, an IR must be performed.

MEMORY PROTECTION REGISTERS

Storage Protection Register (SPR)

20	19	18	17	16	15	0
I	OR	OW	IA	IR	R	

Displacement Value

Use Interrupt B&S Registers during Indirect Addressing*†

Allow Indirect Addressing*

Allow Operand Writing*

Allow Operand Reading*

Allow Instruction Execution*

*Operation Allowed if Bit is Set

Segment Identification Register (SIR)

20	19 17	16	15	0
	SIR_s		SIR_d	

16 Bit Displacement

Base Register Designator

† For complete description of all possible uses, consult the equipment specification NAVSHIPS 0967-051-6291, also, see notes under repeat and indirect addressing tables.

BREAKPOINT REGISTER

19	18	17 Comparison Address Bits 0
0	0	—Disabled
0	1	—Instruction address*
1	0	—Operand address*
1	1	—Instruction and operand addresses*

* An instruction breakpoint match is obtainable on the operand address of a conditional jump instruction, satisfied or unsatisfied. The breakpoint compare is done on the address as it is requested. When a jump instruction is executed the jump address will be requested: (and the breakpoint match will occur) whether the jump condition is met or not.

The P-storage of a satisfied instruction breakpoint interrupt on the operand address of a jump instruction will be the P address of the jump instruction: which did not complete due to the interrupt.

An Instruction or Operand Breakpoint Interrupt occurring on a remotely executed instruction will store the Address of the Execute Remote instruction at CMR 144 (P-storage DSW).

FIXED POINT OVERFLOW CONDITIONS

a) Addition: Addend and augend have like signs and the sum has a different sign.

b) Subtraction: Minuend and subtrahend have different signs and the difference has a sign different from the minuend.

c) Division: Attempt to divide by zero or if the magnitude of divisor times 2^{31} is less than the magnitude of the dividend.

d) Square Root: Attempt to take square root of a negative number or a number greater than or equal to 2^{62}.

INTERRUPT STATUS CODES

(In Descending Priority)

Class	INTERRUPT	Status Code Bits** 9 8 7 6 5 4 3 2 1 0	Action Taken
I*	Power Tolerance (never locked out)	0 0 0 0 0 0 1 1 1 1	(ASR)→CMR141 ISC→CMR142 (P)→CMR143 (CMR140)→P Set ASR bits 19, 14-8. Clear bits 6-0. Bit 7 is unchanged.
I	CP—Operand Memory Resume↙	0 0 M M M M 0 0 0 0	(ASR)→CMR141
I	CP—IOC Command Resume↙	K K 0 0 0 0 0 0 0 1	ISC→CMR142
I	CP—Instruction Memory Resume↙	0 0 M M M M 0 0 1 0	(P)→CMR143
I	CP—IOC Interrupt Code Resume↙	K K 0 0 0 0 0 0 1 1	NDRO Address 000$_8$→P
I*	IOC Memory Resume	K K M M M M 1 0 1 0	Set ASR bits
I*	Intercomputer Timeout	K K C C C C 1 0 1 1	19, 14-8, 7. Clear bits 6-0.
II*	Interprocessor Interrupt	0 0 0 0	(ASR)→CMR145
II	Floating Point Error↙	0 0 0 1	ISC→CMR146
II	CP Illegal Instruction Error‡↙††	0 0 1 0	(P)→CMR147

II	Privileged Instruction Error↙††	0 0 1 1	(CMR144)→P
	Not Assigned	0 1 0 0	Set ASR bits 18,
II	Operand Breakpoint Match†,†	0 1 0 1	13-8. Clear bits
II	Operand Read or Indirect Addressing↙	0 1 1 0	6-0. ASR bit 7
	Not Assigned	0 1 1 1	set only if per-
	Not Assigned	1 0 0 0	forming AUTO REC.
II	Operand Write↙	1 0 0 1	Otherwise bit 7
II	Operand Limit↙	1 0 1 0	is unchanged.
II	Instruction Breakpoint Match↙†	1 0 1 1	
	Not Assigned	1 1 0 0	
II	Instruction Execute ↙††	1 1 0 1	
II	Instruction Limit↙	1 1 1 0	
II*	CP Monitor Clock	1 1 1 1	
III*	IOC Illegal CAR Instruction	K K 0 0 P P 0 0 0 0	(ASR)→CMR151
III*	IOC Illegal Chain Instruction	K K C C C C 0 1 F F	ISC→CMR152
III*	IOC CP Interrupt	K K 0 0 0 0 1 0 1 1	(P)→CMR153
III*	IOC Monitor Clock	K K 0 0 0 0 1 0 1 0	(CMR150)→P
III*	IOC External Interrupt Monitor	K K C C C C 1 1 0 0	Set ASR bits 17, 12-8.
III*	IOC External Function Monitor	K K C C C C 1 1 0 1	Clear bits 6-0.
III*	IOC Output Data Monitor	K K C C C C 1 1 1 0	Bit 7 is unchanged.
III*	IOC Input Data Monitor	K K C C C C 1 1 1 1	
IV	Executive Return	ISC = sy + $(B)_b$ Z.E. 16 bit ISC assigned thru software	(ASR)→CMR155 ISC→CMR156 (P)→CMR157 (CMR154)→P Set ASR bits 16, 11-8. Clear bits 6-0. Bit 7 is unchanged.

INTERRUPT STATUS CODES (continued)

* Queued

** Definitions: PP—CPU NO. (0-2)
MMMM—Memory Bank (0-17)
CCCC—IOC Channel (0-17)
KK—IOC NO. (0-3)

FF = 00—EXT. INT.
01—EXT. FCT.
10—OUTPUT
11—INPUT

‡ If in Interrupt Mode and AUTO REC switch selected, then jump to NDRO address:
01 if bootstrap 0 selected
02 if bootstrap 1 selected
03 if bootstrap 2 selected

† Maintenance Console Breakpoint Program/Manual switch must be in the PROGRAM position.

✓ Stored P value is the address of the instruction causing the interrupt. (Exception - If the processor is executing an instruction while in the repeat mode, the stored P value will be the address of the repeat instruction.)

†† Fault conditions which illuminate program fault light.

For all Class IV, Class III and Class I or II not denoted above, the Stored P value is the address of the next instruction in the interrupted program. (Exception - if the processor is executing an instruction while in the repeat mode, the stored P value will be the address of the repeat instruction.)

ROUNDING OF FLOATING POINT RESULTS

Mantissa rounding is performed ($A_a + 1$) according to the status of the intermediate double-length result in the arithmetic section for add, subtract and multiply; and according to the value of the remainder in divide operations. The final sum or difference mantissa in ($A_a + 1$) is rounded as follows:

1. If bit 31 of the 64 bit intermediate sum or difference equals 1 and ($A_a + 1$) are positive, 1 is added to ($A_a + 1$).
2. If bit 31 of the 64 bit intermediate sum or difference equals 0 and ($A_a + 1$) are negative, 1 is subtracted from ($A_a + 1$).
3. If not 1 or 2 above, ($A_a + 1$) are not changed.
4. If overflow results in 1 or 2 above ($A_a + 1$) are shifted right one place, 1 is added to the characteristic exponent in A_a and the mantissa sign bit in $A_a + 1$ is restored.

Rounding of a product mantissa is done before final sign correction.

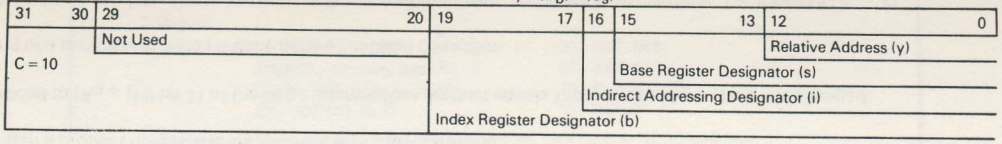
1 is added to ($A_a + 1$) if bit 31 of the 64 bit intermediate product equals 1; otherwise ($A_a + 1$) are not changed.

Rounding of a quotient mantissa is done before final sign correction.

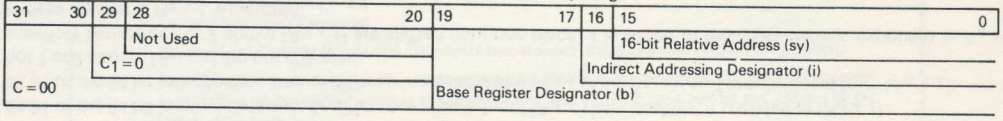
1. If the remainder is equal to or greater than one-half the divisor and there is no overflow, 1 is added to ($A_a + 1$).
2. If bit 31 of the quotient in $A_a + 1$ equals 1, ($A_a + 1$) are shifted right one place, $(A_a + 1)_0$ before shifting, is added to the shifted ($A_a + 1$) and 1 is added to the characteristic exponent in A_a.

INDIRECT ADDRESSING FORMATS

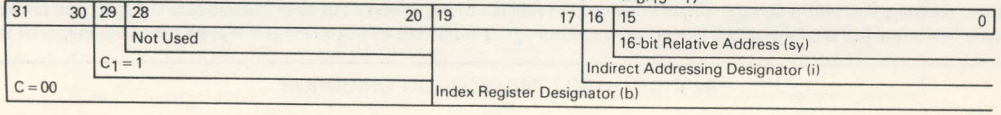
NORMAL (IW) $Y = y + (B_b) + (S_s)$



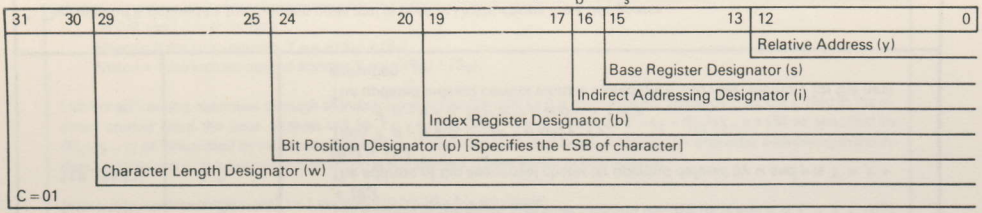
SPECIAL BASE (IWS) $Y = sy + (S_b)$



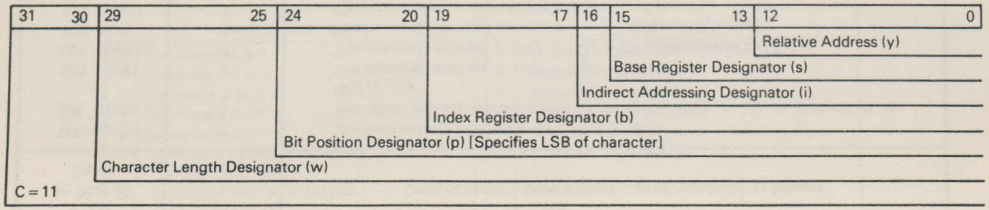
SPECIAL INDEX (IWB) $Y = sy + (B_b)_{15-0} + (S_{(B_b)_{19-17}})$



CHARACTER (IWC) $Y = y + (B_b) + (S_s)$



CHARACTER INCREMENT (IWCI) $Y = y + (B_b) + (S_s)$ Each reference: $(p) - (w) \rightarrow p$. If $(p) - (w) < 0$, then $32 - (w) \rightarrow p$ and $y + 1 \rightarrow y$.



INDIRECT WORD ADDRESS GENERATION

If Bits 31, 30 & 29 Equal	and *i* Equals	Designators in current indirect control word used as follows:
000 (IWS)	1	The next indirect word address $Y = sy + (S_b)$
001 (IWB)	1	The next indirect word address $Y = sy + (B_b) + (S)$ as designated by $(B_b)_{19-17}$
000 (IWS)	0	The operand* address $Y = sy + (S_b)$
001 (IWB)	0	The operand* address $Y = sy + (B_b) + (S)$ as designated by $(B_b)_{19-17}$
10X (IW)	1	The next indirect word address is $Y = y + (B_b) + (S_s)$
01X (IWC)	1	The next indirect word address is $Y = y + (B_b) + (S_s)$
11X (IWCI)	1	The next indirect word address is $Y = y + (B_b) + (S_s)$
10X (IW)	0	The operand* address $Y = y + (B_b) + (S_s)$
01X (IWC)	0	The address of the single character operand defined by w and p is $Y = y + (B_b) + (S_s)$
11X (IWCI)	0	The address of the sequential character operand defined by w and p is $Y = y + (B_b) + (S_s)$. Then if $p - w \geq 0$, $p - w \rightarrow p$ and $y \rightarrow y$ if $p - w < 0$, $32 - w \rightarrow p$ and $y + 1 \rightarrow y$ The updated indirect control word is stored back into main memory for the next execution.

* The operand is defined by the function code and in Format I instructions the *k* designator.

OPERAND INTERPRETATIONS FOR JUMP INSTRUCTIONS (FORMAT III)

z is not used (must be zero

When i = 0 the jump address $Y = y + (B_b) + (S_s)$

When i = 1 the indirect control address $Y = y + (B_b) + (S_s)$.

Indirect addressing continues through all indirect control words until i = 0 is encountered. Depending on the c-field in the indirect control word the jump address will be $Y = y + (B_b) + (S_s)$, $Y = sy + (S_b)$ or $Y = sy + (B_b)_{15-0} + (S)$ as specified by $(B_b)_{19-17}$ as designated by those respective fields in the indirect control word. A request for character addressing in the indirect control word for a Format III instruction is not allowed. These are jump instructions.

Note: Any jump instruction with i = 1 and $(SPR)_S$ bit 16 = 1 is privileged.

REPEAT TERMINATE CONDITIONS

a	Non-Compare Instructions
0	Terminate if A ≠ 0
1	Terminate if A = 0
2	Terminate if A ≥ 0
3	Terminate if A < 0
4	Do not terminate
5	Terminate if (A) is even parity on write into memory
6	Terminate if (A) is odd parity on write into memory
7	Do not terminate

a	Compare Instructions
0	Terminate if CD set to ≠
1	Terminate if CD set to =
2	Terminate if CD set to >
3	Terminate if CD set to ≥
4	Terminate if CD set to <
5	Terminate if CD set to ≤
6	Terminate if CD set to outside limit
7	Terminate if CD set to within limit

REPEAT CONDITIONS (X FOR USABLE)*

Repeated Instruction	a Field of Repeat Inst. 0	1	2	3	4	5	6	7	Terminate on
01 0	X	X	X	X	X			X	A_a
01 1	X	X	X	X	X			X	A_a
01 2	X	X	X	X	X			X	A_{a+1}
01 3	X	X	X	X	X			X	A_a
01 4	X	X	X	X	X			X	A_{a+1}
01 5	X	X	X	X	X			X	A_a
01 6	X	X	X	X	X			X	A_{a+1}
01 7	X	X	X	X	X			X	A_{a+1}
02 0	X	X	X	X	X			X	A_a
02 4	X	X	X	X	X	X	X	X	OP**
02 5	X	X	X	X	X	X	X	X	A_{a+1}
02 6	X	X	X	X	X	X	X	X	A_{a+1}
03 0‡	X	X	X	X	X	X	X	X	A_a
03 1‡	X	X	X	X	X	X	X	X	A_a
03 2‡	X	X	X	X	X	X	X	X	A_{a+1}
03 3‡	X	X	X	X	X			X	A_a
03 4‡	X	X	X	X	X	X	X	X	A_{a+1}
03 5‡	X	X	X	X	X	X	X	X	A_{a+1}
03 6‡	X	X	X	X	X	X	X	X	A_{a+1}

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Repeated Instruction	a Field of Repeat Inst. 0	1	2	3	4	5	6	7	Terminate on
03 7‡	X	X							CD
10	X	X	X	X	X			X	A_a
12	X	X	X	X	X			X	A_{a+1}
13	X	X	X	X	X			X	A_a
14	X	X	X	X	X			X	A_a
15	X	X	X	X	X			X	A_{a+1}
16	X	X	X	X	X			X	A_a
17	X	X	X	X	X			X	A_a
20					X			X	
21					X			X	
22					X			X	
23					X			X	
24	X	X	X	X	X	X	X	X	A_a
26					X	X	X	X	OP**
27					X	X	X	X	OP**
32‡					X			X	
33‡					X			X	
34‡	X	X	X	X	X	X	X	X	A_{a+1}
35‡	X	X	X	X	X	X	X	X	A_a
36‡	X	X	X	X	X	X	X	X	A_{a+1}
37‡	X	X	X	X	X	X	X	X	A_a
40					X			X	
41					X			X	
42	X	X							CD
44	X	X	X	X	X	X			CD
45							X	X	CD
46	X	X	X	X	X	X			CD
47	X	X	X	X	X	X			CD
54†					X			X	
55†					X			X	
56†					X			X	
57†					X			X	

* Unpredictable operation will occur for unusable conditions.

** OP is the 32-bit result of the execution.

† In the repeat mode, ak + 1→ak for each execution. These instructions are <u>not</u> interruptable in the repeat mode. These instructions are privileged if repeat is attempted in the Task mode (Privileged Instruction Error).

‡ For replace class instructions, use S6 on store cycle; if in repeat instruction, b ≠ 0.

Note: Any repeated instruction with i = 1 and $(SPR)_S$ bit 16 = 1 is privileged.
If B7 = Ø skip next instruction.
At termination, sy sign extended will have been added to (B_b).

I/O CONTROLLER INSTRUCTIONS

(All Unused Function Codes are Illegal)

Code	Mnemonic	NAME	DESCRIPTION	UF**	Time μS
10	IB	Initiate Input Buffer on Cj	(y)→CMA* 0 + j; Activate Input	1	3.25
11	OB	Initiate Output Buffer on Cj	(y)→CMA* 20 + j; Activate Output	1	3.25
12	FB	Initiate External Function Buffer on Cj	(y)→CMA* 40 + j; Activate EF	1	3.25
13	XB	Initiate External Interrupt Buffer on Cj	(y)→CMA* 60 + j; Activate EI	1	3.25
14 k = 0	TIB†	Terminate Input Buffer on Cj	Terminate Input { m = 0 Suppress	2	3.0
14 k = 1	TOB†	Terminate Output Buffer on Cj	Terminate Output { Queued Interrupt;	2	3.0
14 k = 2	TFB†	Terminate External Function Buffer on Cj	Terminate EF { m = 1 Allow Queued	2	3.0
14 k = 3	TXB†	Terminate External Interrupt Buffer on Cj	Terminate EI { Interrupt	2	3.0
15 k = 0	IMIR	Set Input Monitor Interrupt Request on Cj	Set Input Monitor Interrupt on Chan j	3	2.5
15 k = 1	OMIR	Set Output Monitor Interrupt Request on Cj	Set Output Monitor Interrupt on Chan j	3	2.5
15 k = 2	FMIR	Set EF Monitor Interrupt Request on Cj	Set EF Monitor Interrupt on Chan j	3	2.5
15 k = 3	XMIR	Set EI Monitor Interrupt Request on Cj	Set EI Monitor Interrupt on Chan j	3	2.5
16 k = 0	AIC	Set Input Chain Active on Cj	y→Command Address Pointer Field	4	2.5
16 k = 1	AOC	Set Output Chain Active on Cj	(bits 55-38) of CMA* 20k + j;	4	2.5
16 k = 2	AFC	Set External Function Chain Active on Cj	Activate Chain	4	2.5
16 k = 3	AXC	Set External Interrupt Chain Active on Cj		4	2.5

17 m = 0	TBZ	Test Bit Zero	If $(y)_{kj} = 0$, SKIP; Else NI	7	4.0
17 m = 1	TBS	Test Bit Set	If $(y)_{kj} \neq 0$, SKIP; Else NI	7	4.0
20	JIO	Jump to y	y→Command Address Pointer or CAR‡	6	2.5
22	LICM	Load IOC Control Memory	(y)→IOC Control Memory Address kj	5	3.25
23	ILTC	Load Real-Time Clock	(y)→Real Time Clock	6	4.0
24	SICM	Store IOC Control Memory	$(\text{IOC Control Memory})_{kj}$→y	5	2.75
25	IBS	Set Bit	1→y_{kj}	5	3.25
26	IBZ	Clear Bit	0→y_{kj}	5	3.25
27	ITSF	Test and Set Flag	1→y_{31}; If $(y)_{31}$ was Originally Cleared, Skip; Else NI	6	3.25
FORMATTING MNEMONICS					
—	BCW	Buffer Control Word		8	—
—	BCWE	Buffer Control Word ESI		9	—

‡ Command Address Register
* Control Memory Address

**ULTRA FORMAT

1—j, y, k, c, m	4—j, y, c	7—kj, y	(l = buffer length)
2—j, c, m	5—kj, y, c	8—y, l	
3—j, c	6—y, c	9—y, l, k	

K-DESIGNATOR

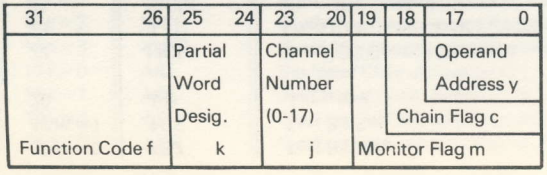
k—DESIGNATOR DEFINITIONS

	k = 0	k = 1	k = 2	k = 3
f = 10, 11, 13	Suppress data	Pack Quarter word	Pack Half word	Whole word
f = 12	Force One Word (y) is EF	One Word Buffer (y) is EF	Multi Word Buffer	Not Used

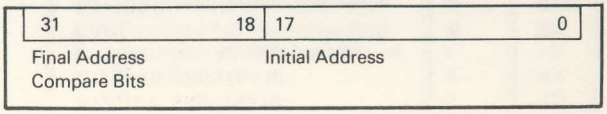
† The terminate buffer commands terminate only active buffers. They have no effect on active chains. Terminating an active buffer also terminates the chain since the buffer never completed normally. To terminate an active chain, it is recommended that a JIO instruction with no chaining be initiated on the channel & function to be terminated (y may be any valid address). However, attempts to terminate a chain on a channel and function with an active buffer will result in the CAP being overlayed but no change to the chain bit in IOCM. In this case, the buffer will complete normally and chaining will commence with the JIO instruction which then terminates the chain.

Note: Clearing the IOC enables all monitor interrupts to all CPU's (i.e., all bits set in all ILR's) and clears all requests.

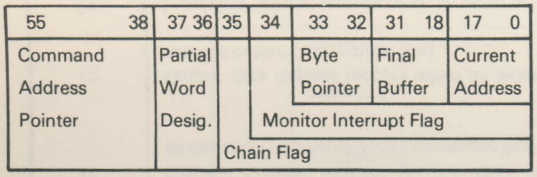
IOC COMMAND WORD FORMAT



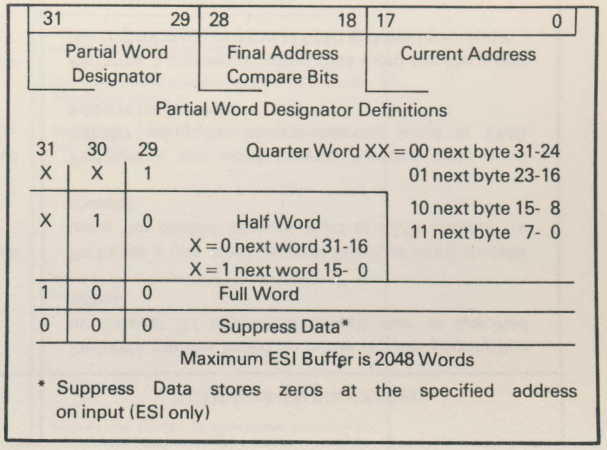
NORMAL BUFFER CONTROL WORD FORMAT



IOC CONTROL MEMORY WORD FORMAT



ESI BUFFER CONTROL WORD FORMAT



* Suppress Data stores zeros at the specified address on input (ESI only)

IOC CONTROL MEMORY ASSIGNMENT

Address	Assignment
0-17	Input
20-37	Output
40-57	External Function
60-77	External Interrupt

IOC BUFFERED REQUEST PRIORITY

REQUEST PRIORITY	REQUEST TITLE	ACTION WHEN PROCESSED
Channel dependent	Buffer request (includes EI, EF, outputs and input)	Performs transfer based on buffer request priority first by channel (17 highest, 0 lowest) then as specified below.
1a	External interrupt request (occurs when an external device sets the external interrupt request line)	Performs a one word external interrupt word transfer using the control memory word at CMR address for channel.
1b	External function request (occurs when an external device sets the external function request line)	Performs a one word external function code word transfer using the control memory word at CMR address for channel.
1c	Output data request (occurs when an external device sets the output data request line)	Performs a one word output data word transfer using the control memory word at CMR address for channel.
1d	Input data request (occurs when an external device sets the input data request line)	Performs a one word input data word transfer using the control memory word at CMR address for channel.

IOC REQUEST (NONBUFFERED) PRIORITY

PRIORITY REQUEST	REQUEST TITLE	ACTION WHEN PROCESSED
1	Intercomputer Terminate Sequence	Performs the termination functions when an intercomputer channel terminates.
2	Clock Request	Decrement the IOC monitor clock by 1 and increment the real-time clock by 1.
3	Central Processor Instruction for IOC and Interrupt Status Code Requests.	Performs the function as commanded according to priority below.
3a	CP No. 0 Request*	
3b	CP No. 1 Request*	
3c	CP No. 2 Request*	
4	Central Processor Command Address Request	Performs the function as commanded according to priority below.
4a	CP No. 0 Request	
4b	CP No. 1 Request	
4c	CP No. 2 Request	
5	Chain Commands (Note 1) (channel associated)	Performs the function as commanded according to normal channel priority.

* The numbers 1 & 2 are IOC port numbers and not necessarily the same as CPU I.D.

Note 1: For buffer terminations with the chain bit (IOCM 35) set, normal priority is bypassed and the next sequential command in that chain is executed.

IOC MAINTENANCE CONSOLE DISPLAY

REGISTER SELECT	CM ADDRESS SELECT/SELECT 2	I/O CONTROLLER DISPLAY (IOC must be in SEQ mode)	MON/ CHAIN
CMP	0-77	Bits 55-38 of IOCM (CAP) specified by CM ADDRESS SELECT	N.U.
CMU	0-77	Bits 37, 36 and 33-18 of IOCM specified by CM ADDRESS SELECT	bit 35 (chain)
CML	0-77	Bits 17-0 of IOCM specified by CM ADDRESS SELECT	bit 34 (monitor)
DIRU	N.U.	Bits 31-18 of DIR	N.U.
DIRL	N.U.	Bits 17-0 of DIR	N.U.
SEL 2	CAR + 0	(CAR 0) bits 17-0‡	CAR ACT.
	CAR + 1	(CAR 1) bits 17-0‡	CAR ACT.
	CAR + 2	(CAR 2) bits 17-0‡	CAR ACT.
	ILR + 0	(ILR 0) channels 15-0†	N.U.
	ILR + 1	(ILR 1) channels 15-0†	N.U.
	ILR + 2	(ILR 2) channels 15-0†	N.U.
	CHAN + 0	Buffer actives by type on channels 3-0†	N.U.

	CHAN + 1	Buffer actives by type on channels 7-4 †	N.U.
	CHAN + 2	Buffer actives by type on channels 10-13†	N.U.
	CHAN + 3	Buffer actives by type on channels 17-14†	N.U.
	CHAIN + 0	Chain actives by type on channels 3-0 †	N.U.
	CHAIN + 1	Chain actives by type on channels 7-4 †	N.U.
	CHAIN + 2	Chain actives by type on channels 13-10†	N.U.
	CHAIN + 3	Chain actives by type on channels 17-14†	N.U.
	60	(RTC) bits 17-0	CAR 0 ACTIVE
	61	(RTC) bits 31-18	CAR 1 ACTIVE
	62	(IOC MONITOR CLK) 15-0	N.U.

N.U. Not Used

† These displays are indicate only and are available in both RUN and SEQ mode.

‡ These displays are available in both RUN and SEQ mode.

512-WORD NDROs (Part No. 7074003-XXX)

NDRO NO.	CPU NO.	NORMAL IOC	ALT. IOC	PERIPHERAL DEVICE	CHAN. NO.	ADDRESS WSBA
66	0	0	1	DEAC MT	13	000020 and
				DEAC PT	13	100020
	1	0	1	DEAC MT	13	140020 and
				DEAC PT	13	240020
	2	0	1	DEAC MT	13	300020 and
				DEAC PT	13	400020
	3	0	2	DEAC MT	13	640020 and
				DEAC PT	13	740020
70	Note 1	0	None	DEAC MT	16	000007
				DEAC PT	16	
74	Note 1	0	None	MT	0	000007
				RD-281(V)	17	
77	Note 1	1	None	DEAC MT	13	000007
				DEAC PT	13	
85	Note 1	0	None	MT	13	000007
				PT	13	
86	Note 1	0	None	MT	1	000007
				PT	0	
87	Note 1	0	None	MT	13	000007 and
				PT	11	040007
88	Note 1	0	None	MT	1	000007
				RD-281(V)	17	
89	Note 1	0	None	MT	15	000007
				PT	0	

NDRO NO.	CPU NO.	NORMAL IOC	ALT. IOC	PERIPHERAL DEVICE	CHAN. NO.	ADDRESS WSBA
102	Note 1	1	None	DEAC MT	13	340007
				RD-358(V)/UYK MT	14	
103	Note 1	0	None	TACC Mag. Tape	15	000007
				TACC Disk File	16	
104	Note 1	1	None	TACC Mag. Tape	15	000007
				TACC Disk File	16	
105	0	0	1	MT	3	000020 and
				RD-281(V)2	17	100020
	1	1	0	MT	3	200020 and
				RD-281(V)2	17	300020
106	Note 1	0	None	RD-358/UYK MT 9-Trk	1	000007
				PT	0	
107	Note 1	1	None	RD-358 MT 7-Trk	1	000007
				RD-281(V)2	17	
108	Note 1	1	None	MT	15	000007
				PT	1	
109	Note 1	0	None	DEAC MT	4	000007 and
				DEAC PT	4	040007
110	Note 1	0	None	RD-358 MT 9-Trk 800 bpi	15	000007
				PT	0	
111	Note 1	0	None	PT	2	000007
				RD-281(V)2	17	
112	Note 1	0	1	MT	15	000007 and
				RD-281(V)2	17	040007

90	Note 1	0	None	DEAC MT	2	000007
				RD-281(V)2	17	
91	Note 1	0	None	MT	11	000007
				PT	4	
92	Note 1	1	None	DEAC MT	2	000007
				RD-281(V)2	17	
93	Note 1	0	None	MT	5	000007
				PT	4	
94	Note 1	1	None	MT	5	000007
				PT	4	
95	0	0	1	Compunetics Magnetic Tape	3	000020 and
				RD-281(V)2	15	100020
	1	0	1	Compunetics Magnetic Tape	3	140020 and
				RD-281(V)2	15	240020
96	Note 1	0	None	MT	15	000007
				RD-281(V)	17	
98	Note 1	0	None	MT	13	000007 and
				PT	7	040007
99	Note 1	0	None	DEAC MT	13	000007
				DEAC PT	13	
100	0	0	1	DEAC MT	13	000020 and
				DEAC PT	13	100020
	1	0	1	DEAC MT	13	140020 and
				DEAC PT	13	240020
	2	2	3	DEAC MT	13	500020 and
				DEAC PT	13	600020
101	Note 1	0	None	MT	11	000007
				PT	4	

113	Note 1	1	0	MT	15	000007 and
				PT	0	040007
114	Note 1	0	1	PT	0	000007 and
				RD-281(V)2	17	040007
115	0	0	None	RD-358(V) MT 9-Trk	16	000003
				CDC 9760 MUX/MPP Disk File	17	
	1	1	None	RD-358(V) MT 9-Trk	16	240003
				CDC 9760 MUX/MPP Disk File	17	
	2	2	None	RD-358(V) MT 9-Trk	16	400003
				CDC 9760 MUX/MPP Disk File	17	
	3	3	None	RD-358(V) MT 9-Trk	16	700003
				CDC 9760 MUX/MPP Disk File	17	
116	0	0	None	RD-281(V)3 Disk File	17	002007
		1	None	RD-281(V)3 Disk File	17	
	1	0	None	RD-281(V)3 Disk File	17	202007
		1	None	RD-281(V)3 Disk File	17	
	2	0	None	RD-281(V)3 Disk File	17	202007
		1	None	RD-281(V)3 Disk File	17	
117	0	0	None	Potter SC 1051 Mag. Tape	16	000007
				CDC 9742 Disk File	17	
	1	1	None	Potter SC 1051 Mag. Tape	16	200007
				CDC 9742 Disk File	17	
118	0	0	1	MT	10	000007 and
				PT	4	200007
	1	1	0	MT	10	200007 and
				PT	4	000007
119	Note 1	0	1	MT	15	000007 and
				RD-281(V)2	17	100007

512-WORD NDROs (Part No. 7074003-XXX) (continued)

NDRO NO.	CPU NO.	NORMAL IOC	ALT. IOC	PERIPHERAL DEVICE	CHAN. NO.	ADDRESS WSBA
120	Note 1	1	0	MT	15	000007 and
				PT	0	100007
121	Note 1	0	None	Kennedy 9100 w/Datum Contr.	12	000007
				CDC 9760 w/SI Contr.	17	
123	0	0	None	DEAC MT	2	000003
				RD-281(V)3	17	
	1	1	None	DEAC MT	2	000003
				RD-281(V)3	17	
124	0	0	None	1870 Mag. Tape Cassette	13	000007
				1870 Paper Tape Reader	13	
	1	1	None	1870 Mag. Tape Cassette	13	140007
				1870 Paper Tape Reader	13	
125	0	0	None	DEAC MT	0	000007
				DSS+2 (ADF) Disk File	6	
	1	1	None	DEAC MT	0	000007
				DSS+2 (ADF) Disk File	6	
127	Note 1	0	None	Uniservo 16 MT w/MSA Contr.	5	000007
				PT	1	
128	0	0	1	DEAC MT	13	000020 and
				DEAC PT	13	100020
	1	0	1	DEAC MT	13	200020 and
				DEAC PT	13	300020
	2	2	3	DEAC MT	13	640020 and
				DEAC PT	13	740020

NDRO NO.	CPU NO.	NORMAL IOC	ALT. IOC	PERIPHERAL DEVICE	CHAN. NO.	ADDRESS WSBA
139	0	0	1	DEAC MT	13	000007
				DEAC PT	13	
	1	0	1	DEAC MT	13	000007
				DEAC PT	13	
140	Note 1	0	1	MT	11	000007
				DEAC PT	13	
141	Note 1	1	0	DEAC MT	15	000007
				PT	17	
142	0	0	1	MT	10	000007 and
				PT	4	200007
	1	1	0	MT	10	200007 and
				PT	4	000007
	2	0	1	MT	10	400007 and
				PT	4	200007
143	0	0	None	AN/UYH-2(V) Disk (DSS+2)	17	000007
				PT	0	
144	1	1	None	AN/UYH-2(V) Disk (DSS+2)	17	000007
				RD-358(V) MT 7/9-Trk	13	
145	0	0	None	DEAC MT	3	000007 and
				DEAC PT	3	100007
	1	1	None	DEAC MT	3	300007 and
				DEAC PT	3	400007
	0	3	2	RD-281 Disk	17	000020 and
		0	1	DEAC MT	13	100020

129	Note 1	0	None	DEAC MT	3	000007 and
				DEAC PT	3	040007
131	Note 1	0	None	Kennedy 9100 MTU via PCS	7	000007
				UYK-20 Intercomputer	17	
				Quantex CMTU AN/USH-26 MT	6	
132	Note 1	1	None	RD-358(V) MT 7/9-Trk	4	000007
		0	None	CDC 640 Disk Storage Unit	17	
133	0	1	0	MT	11	000007
				PT	17	
	1	1	0	MT	11	000007
				PT	17	
134	Note 1	0	None	RD-358(V) MT 9-Trk	13	000007
				PT	12	
135	0	0	1	DEAC MT	15	000007
				U-1647 Disk	17	
	1	1	0	DEAC MT	15	200007
				U-1647 Disk	17	
136	0	0	1	DEAC MT	15	000007
				Kennedy 9100 MT Datum Contr.	12	
	1	1	0	DEAC MT	15	200007
				Kennedy 9100 MT Datum Contr.	12	
137	Note 1	0	None	RD-358(V) MT 9-Trk	15	000007
				CDC 976X Disk w/SI Contr.	17	
138	Note 1	0	None	RD-358(V) MT 9-Trk	13	000007
				PT	11	

146	1	3	2	RD-281 Disk	17	200020 and
		0	1	DEAC MT	13	300020
	2	2	3	RD-281 Disk	17	640020 and
		2	3	DEAC MT	13	740020
147	0	0	None	1840 7-Trk MT	14	000007 and
				PT	11	200007
	1	1	None	1840 7-Trk MT	14	000007 and
				PT	11	200000
148	0	0	1	Uniservo VIIIC	15	000007 and
				CDC 976X Disk w/SI Contr.	17	300007
	1	1	0	Uniservo VIIIC	15	300007 and
				CDC 976X Disk w/SI Contr.	17	000007
149	0	0	1	Quantex CMTU AN/USH-26 MT	15	000007 and
				AN/UYH-3 Disk	17	000007
	1	1	0	Quantex CMTU AN/USH-26 MT	15	300007 and
				AN/UYH-3 Disk	17	000007
150	Note 1	0	1	RD-358(V) MT 7-Trk	0	000007
				AN/UYH-3 Disk	17	
152	0	0	1	RD-270(V) MT	15	000007 and
				CDC 976X Disk w/SI Contr.	17	100007
	1	1	0	RD-270(V) MT	15	100007 and
				CDC 976X Disk w/SI Contr.	17	000007
153	Note 1	0	None	DEAC MT	13	000007
				DEAC PT	4	
154	Note 1	0	2	AN/UYH-3 Disk	17	000007
		1	None	RD-358(V) MT 7-Trk	12	
155	Note 1	0	None	AN/UYH-3 Disk	17	000007
				RD-358(V) MT 7-Trk	12	

1024-WORD NDROs (Part No. 7217500-XXX)

NDRO NO.	CPU NO.	NORMAL IOC	ALT. IOC	EN-TRANCE	PERIPHERAL DEVICE	CHAN. NO.	ADDRESS WSBA
02	0	0	None	Boot 1	DEAC MT	0	000007
				Boot 2	DSS+2 Disk	0	
				Man. Entr.	PT	0	
	1	1	None	Same	Same	Same	000007
	2	0	None	Same	Same	Same	000007
	3	1	None	Same	Same	Same	000007
	4	1	None	Same	Same	Same	000007
	5	1	None	Same	Same	Same	000007
	6	2	None	Same	Same	Same	000007
	7	1	None	Same	Same	Same	000007
05 Note 4	0	0	1	1	DEAC MT	12	000007
				1	DEAC PT	12	
				2	U-1647 Disk	11	
	1	0	1	1	DEAC MT	13	200007
				1	DEAC PT	13	
				2	U-1647 Disk	11	
06	0 Note 4	0	None	1	AN/UYH-3 Disk	17	000007
				1	AN/USH-19 MT	5	
				2	RD-358 MT (9-Trk)	16	
				2	PT	4	
	1	1	None	Same	Same	Same	000007
07	Note 4 Note 5	0	None	1	DEAC MT	10	000007 and 100007
				1	DEAC PT	10	
				2	AN/UYH-2 Disk	13	

NDRO NO.	CPU NO.	NORMAL IOC	ALT. IOC	EN-TRANCE	PERIPHERAL DEVICE	CHAN. NO.	ADDRESS WSBA
14		0	None	1	AN/UYH-3 Disk	12	000007 and 100007
		0	None	2	RD-358(V) MT 9-Trk	13	
		1	None	Man. Entr.	AN/USH-19 MT	10	
		1	None	Man. Entr.	PT	4	
15	Note 1	0	1	1	Kennedy 9100 w/Datum Contr.	12	000007
				2	CDC 976X w/SI Contr.	17	
16 Note 3 Note 4	0	0	None	1	RD-358 MT	11	000007
				1	AN/USH-26 MT	3	
				2	CDC 976X Disk w/SI Contr.	7	
				Man. Entr.	PT	4	
17	Note 1	0	None	Boot 1	RD-358 MT 7-Trk.	14	000007 and 100007
				Boot 2	RD-281(V)2 Disk	17	
18	0	0	None	Boot 1	RASS Disk	17	000007
				Boot 1	DEAC MT	0	
				Boot 2	DSS+2 Disk	0	
	1	1	None	Same	Same	Same	000007
	2	0	None	Same	Same	Same	000007
	3	1	None	Same	Same	Same	000007
	4	1	None	Same	Same	Same	000007
	5	1	None	Same	Same	Same	000007
	6	2	None	Same	Same	Same	000007
	7	1	None	Same	Same	Same	000007
19	Note 1	0	None	Boot 1	ROLM 1602B/MILTOPE	0	777500
				Boot 2	RD-448 Disk	17	

08	0	0	None	1	DEAC MT	13	000007
				1	PT	11	
				2	DEAC PT	13	
				2	RD-358 MT 7-Trk	13	
	1	1	None	Same	Same	Same	000007
09 Note 3 Note 4	0	0	None	1	1840 MT	11	000007
				1	AN/USH-26 MT	3	
				2	CDC 976X Disk w/SI Contr.	7	
				Man. Entr.	PT	4	
10 Note 4	0	0	1	1	Quantex CMTU AN/USH-26 MT	4	000007 and 300007
				1	DEAC MT	13	
				2	RD-358(V) MT 7-Trk	14	
				2	CDC 9762 Disk w/SI Contr.	17	
	1	1	0	1	Quantex CMTU AN/USH-26 MT	4	300007 and 000007
				1	DEAC MT	13	
				2	RD-358(V) MT 7-Trk	14	
				2	CDC 9762 Disk w/SI Contr.	17	
11	Note 1	0	None	1	MT	7	000007
		1	None	2	Quantex CMTU AN/USH-26 MT	7	
		1	None	1	MT	13	
		0	None	2	Quantex CMTU AN/USH-26 MT	13	
12	0	0	1	1	AN/UYH-3 Disk	17	000020 and 200020
				2	AN/USH-19 MT	13	
	1	1	0	1	AN/UYH-3 Disk	17	240020 and 400020
				2	AN/USH-19 MT	13	
	2	0	1	1	AN/UYH-3 Disk	17	500020 and 700020
				2	AN/USH-19 MT	13	
13	Note 1	0	None	1	RD-358(V) MT 9-Trk	13	000007
				2	CDC 9766 Disk w/SI Contr.	17	

ABBREVIATIONS AND NOTES

ALT. REC.	Alternate Recovery
DEAC MT	OJ-172(V)
DEAC PT	OJ-172(V)
ICW	Interrupt Control Word
MT	RD-270, RD-294(V), 1840, or 1840M (7-track) Magnetic Tape
PCS	Peripheral Controller System
PT	OA-7984(V), 1538 Paper Tape
RD-281(V)	Nonduplexed RD-281
RD-281(V)2	Duplexed or Nonduplexed RD-281
S0	Base Register 0
WSBA	Working Storage Base Address

Note 1: This NDRO will function with parameters as shown in CPU Nos. 0, 1, 2, or 3.

Note 2: Provided with Interrupt Switcher Program which provides an additional three alternate recovery entrance addresses.

Note 3: This NDRO design also includes boot write programs for the MT and AN/USH-26(V) peripherals.

Note 4: This NDRO design uses special Jump Key Settings to differentiate between peripherals attached to same boot entrance switch.

Note 5: This NDRO design also includes a boot write program for the AN/UYH-2 (DSS+2) disk.

Note 6: This NDRO design allows for the contents of S0 to be variable address under software control.

NOTE 7: This NDRO design uses boot 1 switch to load from a Miltope Tape Unit using OA-7984(V) Paper Tape Load Scenario.

I/O MODE SELECTORS

Part No. 7073230	Channel Modes				IC Timeout (Millisec.)	Rotation of Priority
	Normal	ESI	ESA	Intercomputer		
-00	Unassembled Parts Only					
-01	0-17					
-02	2-17			0, 1	1000	Group 0
-03	2-17			0, 1	250	Group 0
-04	0-15, 17			16	250	Group 3
-05	4-17			0-3	1000	Group 0
-06	0-11			12-17	250	Groups 2, 3
-07	0-11, 13-15, 17			12, 16	250	Groups 2, 3
-08	4-17			0-3	250	Group 0
-09	0-7, 11, 13-17			10, 12	250	
-10	0-11, 13-17			12	250	
-11	0, 2-11, 14-17	12, 13		1	250	
-12	0-7, 14-17			10-13	250	
-13	1-17			0	250	
-14	0-15, 17			16	250	
-15	1-17			0	500	Group 0
-16	3-17			0-2	250	Group 0
-17	0-1, 6-17			2-5	250	Group 0
-18	0-3, 5-7, 11, 13-17	4, 12		10	250	
-19	4, 10-17			0-3, 5-7	250	Groups 0, 1

Part No. 7073230	Channel Modes				IC Timeout (Millisec.)	Rotation of Priority
	Normal	ESI	ESA	Intercomputer		
-39	0-7, 11-13			10, 14-17	250	
-40	0, 1, 4-17			2, 3	1000	
-41	0, 1, 3, 4, 15, 16, 17			2, 5-14	250	
-42	0, 1, 2, 4, 15, 16			3, 5-14, 17	250	
-43	10-17			0-7	250	Groups 0, 1
-44	1-15, 17			0, 16	250	
-45	4-17			0-3	250	
-46	10-12, 15-17			0-7, 13, 14	250	Groups 0, 1
-47	4, 10-17			0-3, 5-7	250	Groups 0, 1
-48	0-7, 11, 13-17	12		10	250	
-49	4-6, 10-17			0-3, 7	250	Group 0
-50	0-5, 12-17			6, 7, 10, 11	250	Group 1
-51	1-3, 12-17			0, 4-11	250	
-52	0-2, 5, 6, 14-17			3, 4, 7-13	250	
-53	0-2, 4-6, 10-11, 14-17			3, 7, 12, 13	250	
-54	0-2, 4-6, 14-17			3, 7-13	250	
-55	2, 3, 5-7, 14-17			0, 1, 4, 10-13	250	

-20	0-7, 11, 13-17			10, 12	250	Group 2
-21	2-17			0, 1	500	Group 0
-22	0-11, 14-16	12, 13, 17				
-23	2, 3, 6-17			0, 1, 4, 5	250	Groups 0, 1
-24	6-17			0-5	250	Groups 0, 1
-25	1-17			0	250	Group 0
-26	2-14	15, 16, 17		0, 1	250	Group 0
-27	4-17			0-3	500	Group 0
-28	0-3, 10-17	4-7				
-29	17, 2-4, 7, 12, 14, 16			0, 1, 5, 6, 10, 11, 13, 15	250	Group 2
-30	1-3, 5-17			0, 4	250	Groups 0, 1
-31	0, 2-17			1	1000	
-32	0-3, 5-11, 14-17			4, 12, 13	250	
-33	0-3, 5-7, 14-17			4, 10, 11, 12, 13	250	
-34	0, 11, 15-17			1-10, 12-14	250	
-35	11, 15-17			0-10, 12-14	250	
-36	4, 7, 10, 13-17			0-3, 5, 6, 11, 12	250	Groups 0, 1, 2
-37	0-7, 11, 13-17			10, 12	1000	
-38	0-2, 5, 7-17			3, 4, 6	1000	

-56	0-3, 5, 6, 14-17			4, 7, 10-13	250	
-57	0-2, 4, 15-17			3, 5-14	250	
-58	0-6, 10, 11, 14-17			7, 12, 13	250	
-59	0-4, 6-7, 11-17			5, 10	250	
-60	2-7, 10, 12, 14-17			0, 1, 11, 13	250	Group 0
-61	1-7, 10-12, 14-17			0, 13	250	Group 0
-62	1, 4-17			0, 2, 3	1000	
-63	4, 5, 7-17			0-3, 6	250	Groups 0, 1
-64	4-10, 14, 16	11-13		0-3, 15, 17	250	Groups 0, 3
-65	6-17			0-5	250	Groups 0, 1, 3
-66	0-5, 10-12, 14-17	13		6-7	250	
-67	1-17			0	1000	
-68	0-15			16, 17	250	
-69	0-3, 5-6, 11-12, 14-17			4, 7, 10, 13	250	
-70	1, 3-17			0, 2	250	Group 0
-71	1, 2, 3, 14-17			0, 4-13	250	
-72	0-3, 10-17		4-7			
-73	7-17			0-6	250	Group 0
-74	0, 1, 5-17			2, 3, 4	250	

MODE SELECTORS

I/O MODE SELECTORS (continued)

Part No. 7073230	Channel Modes				IC Timeout (Millisec.)	Rotation of Priority
	Normal	ESI	ESA	Intercomputer		
-75	0-11, 13-17	12				
-76	10-15, 17			0-7, 16	250	
-77	10-13, 15, 17			0-7, 14, 16	250	
-78	3, 5-7, 11-17			0-2, 4, 10	250	Groups 0, 1, 2
-79	4-7, 14, 16	10-13		0-3, 15, 17	250	Groups 0, 3
-80	0-1, 5, 6, 14-17			2, 4, 7-13	250	
-81	3, 5, 10-14	15-17		0-2, 4, 6, 7	250	Groups 0, 1
-82	0-11, 14-17			12, 13	250	
-83	4, 5, 7, 10, 12-17			0-3, 6, 11	500	
-84	4, 5, 7-17			0-3, 6	500	
-85	4-17			0-3	250	Group 0
-86	1-6, 10, 11, 14-17			0, 7, 12, 13	1000	Group 2
-87	1-6, 10, 11, 13-17			0, 7, 12	1000	Group 2
-88	2-5, 7-14	15, 16, 17		0, 1, 6	250	Groups 0, 1
-89	1, 3, 4, 6-11, 14	12, 13, 15-17		0, 2, 5	250	Groups 0, 1
-90	0-7, 11, 14-17			10, 12, 13	250	

Part No. 7073230	Channel Modes				IC Timeout (Millisec.)	Rotation of Priority
	Normal	ESI	ESA	Intercomputer		
-105	3, 4, 7, 10, 13			0-2, 5, 6, 11, 12, 14-17	250	Groups 0, 3
-106	3, 4, 7, 10, 12, 13, 15			0-2, 5, 6, 11, 14, 16, 17	250	Groups 0, 3
-107	3, 4, 7-13, 15			0-2, 5, 6, 14, 16, 17	250	Groups 0, 3
-108	3, 4, 7-10, 12-17			0-2, 5, 6, 11	250	Group 0
-109	3, 4, 7-10, 13-17			0-2, 5, 6, 11, 12	250	Group 0
-110	3-4, 7-11, 13			0-2, 5, 6, 12, 14-17	250	Groups 0, 3
-111	Not Used					
-112	Not Used					
-113	Not Used					
-114	3-13, 15			0, 1, 2, 14, 16, 17	250	Groups 0, 3
-115 thru -124 Not Used						
-125	1, 2, 4, 5, 7-11, 13-15, 17			0, 3, 6, 12, 16	250	Groups 0, 1, 2, 3
-126	1, 2, 4, 6-13	15-17		0, 3, 5, 14	250	Groups 0, 3
-127	3, 5, 10-17			0-2, 4, 6, 7	250	Groups 0, 1, 2, 3
-128	4-14, 16			0-3, 15, 17	250	Groups 0, 3
-129	4, 5, 7, 10, 12-17			0-3, 6, 11	250	

-91	1, 3, 5, 10-17			0, 2, 4, 6, 7	250	Groups 0, 1
-92	2, 3, 5, 7-17			0, 1, 4, 6	250	Groups 0, 1
-93	0-2, 6-17			3, 4, 5	250	
-94	0-14, 17			15, 16	250	
-95	0-12, 14, 15, 17			13, 16	250	Groups 2, 3
-96	0, 1, 4, 5, 10-17			2, 3, 6, 7	250	
-97	0-13, 15, 17			14, 16	250	
-98	4-13, 16			0-3, 14, 15, 17	250	Groups 0, 3
-99	Unwired Assembled					
-100	4-6, 10, 11, 13-15, 17			0-3, 7, 12, 16	250	Group 0
-101	4-6, 10-13, 15, 16			0-3, 7, 14, 17	250	Group 0
-102	4-6, 10-12, 14-17			0-3, 7, 13	250	Group 0
-103	3, 4, 7, 10, 13, 15, 17			0-2, 5, 6, 11, 12, 14, 16	250	Group 0
-104	3, 4, 7, 10, 13, 15			0-2, 5, 6, 11, 12, 14, 16, 17	250	Groups 0, 3

-130	4, 5, 7-17			0-3, 6	250	
-131	1-11, 14-17			0, 12, 13	1000	
-132	5-7, 10-13, 15-17			0-4, 14	250	Groups 0, 1, 2, 3
-133	4-7, 11-17			0-3, 10	250	Group 0
-134	5-17			0-4	250	Group 0
-135	6, 7, 10-17			0-5	250	Group 0
-136	5-7, 10-12, 15-17			0-4, 13, 14	250	Groups 0, 1, 2, 3
-137	2-14, 16, 17	15		0, 1	250	Group 0
-138	0-3, 7, 10-14, 16, 17			4, 5, 6, 15	250	Group 1
-139	1-17			0	1000	Groups 0, 2, 3
-140	4-7, 14, 16			0-3, 10-13, 15, 17	250	Groups 0, 2, 3
-141	1-17			0	1000	Group 3
-142	0-2, 5, 6, 12, 15-17			3, 4, 7, 10, 11, 13, 14	250	
-143	4, 6, 10-17			0-3, 5, 7	250	Groups 0, 1
-144	0-3, 14-17	10, 11	12, 13	4-7	250	Group 1

EF WORD

	EF WORD FUNCTION	CODE AND BIT ASSIGNMENT (15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0)
1	LOAD TRK SELECT	0001 — UNASND — TRACK # — TCC
3	READ	0011 — STARTING BLOCK ADDRESS REG
4	WRITE	0100
6	LOAD BLOCK COUNTER SEND STATUS SUPPRESS INTERRUPT	0110 — NUMBER BLKS READ/WRITTEN
		0111
10	REQUEST STATUS WORDS 1 & 2	1000 — UNASSIGNED
11	WORD 1	1001
12	WORD 2	1010
17	MASTER CLEAR	1111

STATUS WORD ONE

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

- 9–0: CURRENT BLOCK ADDRESS COUNTER CONTENT
- 10: NOT USED
- 11: 0 = NO ILLEGAL TRACK OR EF WORD; 1 = ILLEGAL TRACK OR EF WORD
- 12: 0 = NO MEMORY PROTECT ERROR; 1 = MEMORY PROTECT ERROR
- 13: 0 = NO TIMING ERROR; 1 = TIMING ERROR
- 14: 0 = NO POLYNOMIAL CHECK ERROR; 1 = POLYNOMIAL CHECK ERROR
- 15: 0 = CONTROL ACKNOWLEDGE; 1 = LOSS OF CONTROL

STATUS WORD TWO

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

- 7–0: CURRENT TRACK NUMBER
- 14–8: UNASSIGNED
- 15: 0 = CONTROL ACKNOWLEDGE; 1 = LOSS OF CONTROL

RD-358/1540/1240/USH-19 TAPE UNITS (7 TRACK)

35 ← NOT INTERPRETED → 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

- 1 = Improper Condition
- 1 = No / 0 = Yes } Duplex Control*
- 1 = Transport Selected*
- 1 = XIRG Detected* †
- 1 = Output Timing Error
- 1 = Input Timing Error
- 1 = Incorrect Frame Count
- 1 = Lateral Parity Error
- 1 = Longitudinal Parity Error
- 1 = Backward / 0 = Forward } Last Motion of Tape
- 1 = Tape Mark (End of File)
- 1 = No Write Enable
- 1 = End of Tape
- 1 = Low Tape †
- 1 = Load Point

*RD-358/1540/1541 † Not applicable AN/USH-19

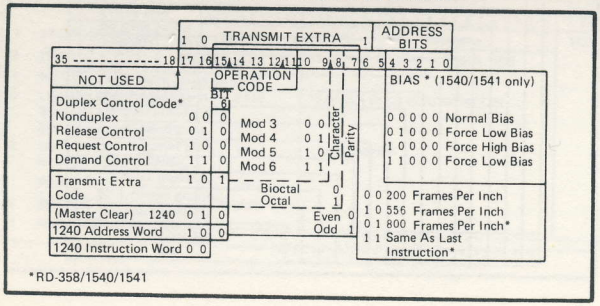
OPERATION CODES

CODE	7-TRACK RD-358/1240 INSTRUCTIONS	7-TRACK RD-358/1540 INSTRUCTIONS	9-TRACK RD-358 INSTRUCTIONS
00000	Read Forward	Read Forward	Read Forward
00001	Read Selective	Read Selective	Read Selective
00010	Read-Ignore Error Halt	Read-Modified Stop	Space Block
00011	Space File	Space File	Space File
00100	Type I Search	Type I Search	Type I Search
00101	Type II Search	Type II Search	Type II Search
00110	Type I Search File	Type I Search File	Type I Search File
00111	Type II Search File	Type II Search File	Type II Search File
01000	Write	Write	Write
01001	Write-XIRG	Write-XIRG	Write-XIRG
01010	Write-Ignore Error Halt	Write-Ignore Error Halt	Write-Ignore Error Halt
01011	Write-XIRG Ignore Error Halt	Write-XIRG Ignore Error Halt	Write-XIRG Ignore Error Halt
01100	Write Tape Mark	Write-Modified Stop	Write-Modified Stop
01101	Write Tape Mark XIRG	Write Edit	Erase
01110	Write Tape Mark	Write Tape Mark	Write Tape Mark
01111	Write Tape Mark XIRG	Write Tape Mark XIRG	Write Tape Mark XIRG
10000	Backspace	Backread	Backread
10001	Backspace	Backread Selective	Backread Selective
10010	Backspace Read	Backread Modified Stop	Backspace Block
10011	Backspace File	Backspace File	Backspace File
10100	Type I Backsearch	Type I Backsearch	Type I Backsearch
10101	Type II Backsearch	Type II Backsearch	Type II Backsearch
10110	Type I Backsearch File	Type I Backsearch File	Type I Backsearch File
10111	Type II Backsearch File	Type II Backsearch File	Type II Backsearch File
11000	Rewind	Rewind	Rewind
11001	Rewind Clear Write Enable	Rewind Clear Write Enable	Rewind Clear Write Enable
11010	Rewind	Rewind	Rewind Interrupt at Load Point
11011	Rewind Clear Write Enable	Rewind Clear Write Enable	Rewind
11100	Rewind Read	Rewind Read	Rewind Read
11101	Rewind Read Clear Write Enable	Rewind Read Clear Write Enable	Reread
11110	Rewind Read	Rewind Read	Rewind Read
11111	Rewind Read Clear Write Enable	Request Status	Request Status
*	Transmit Extra	Transmit Extra	------

*Bits 17, 16, and 6 of Function Word = 101 respectively.

RD-358/1540/1240/USH-19 TAPE UNITS (7 TRACK) (continued)

FUNCTION CODE FORMAT



*RD-358/1540/1541

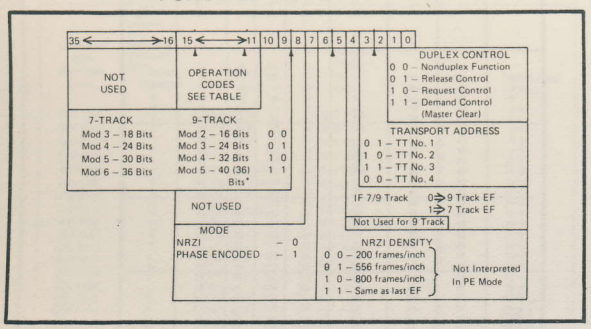
ADDRESS BITS

1540 ADDRESSING						1240 ADDRESSING							
Bit Position					Switch # Position	Bit Position						Cabinet	Switch # Position
4	3	2	1	0		5	4	3	2	1	0		
0	1	X	0	1	1	0	0	1	0	0	1	1	1
0	1	X	1	0	2	0	0	1	0	1	0	1	2
0	1	X	1	1	3	0	0	1	0	1	1	1	3
0	1	1	0	0	4	0	0	1	1	0	0	1	4
1	0	X	0	1	5	0	1	0	0	0	1	2	1
1	0	X	1	0	6	0	1	0	0	1	0	2	2
1	0	X	1	1	7	0	1	0	0	1	1	2	3
1	0	1	0	0	8	0	1	0	1	0	0	2	4
1	1	X	0	1	9	0	1	1	0	0	1	3	1
1	1	X	1	0	10	0	1	1	0	1	0	3	2
1	1	X	1	1	11	0	1	1	0	1	1	3	3
1	1	1	0	0	12	0	1	1	1	0	0	3	4
0	0	X	0	1	13	1	0	0	0	0	1	4	1
0	0	X	1	0	14	1	0	0	0	1	0	4	2
0	0	X	1	1	15	1	0	0	0	1	1	4	3
0	0	1	0	0	16	1	0	0	1	0	0	4	4

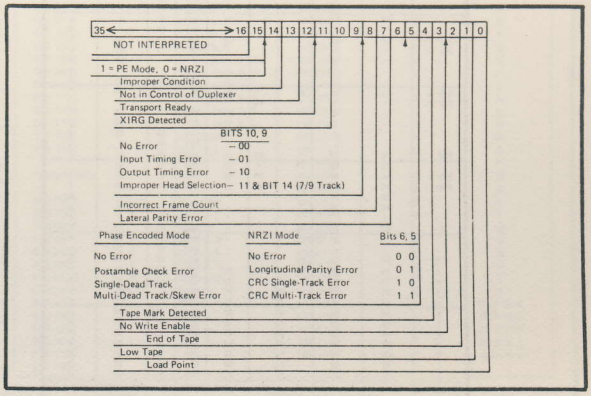
# Indicates position of address switch on each tape transport.
X = zero or one.

RD-358 9 OR 7/9 TRACK

FUNCTION CODE FORMAT



STATUS CODE FORMAT



CHARACTER CODES

Character	1232 I/O Console Field Data	XS-3	ASCII	Teletype	Flexowriter Upper and Lower Case	BCD Tape Character	BCD Character	Card Punch
A	06	24	101	30	30	61	21	12-1
B	07	25	102	23	23	62	22	12-2
C	10	26	103	16	16	63	23	12-3
D	11	27	104	22	22	64	24	12-4
E	12	30	105	20	20	65	25	12-5
F	13	31	106	26	26	66	26	12-6
G	14	32	107	13	13	67	27	12-7
H	15	33	110	05	05	70	30	12-8
I	16	34	111	14	14	71	31	12-9
J	17	44	112	32	32	41	41	11-1
K	20	45	113	36	36	42	42	11-2
L	21	46	114	11	11	43	43	11-3
M	22	47	115	07	07	44	44	11-4
N	23	50	116	06	06	45	45	11-5
O	24	51	117	03	03	46	46	11-6
P	25	52	120	15	15	47	47	11-7
Q	26	53	121	35	35	50	50	11-8
R	27	54	122	12	12	51	51	11-9
S	30	65	123	24	24	22	62	0-2
T	31	66	124	01	01	23	63	0-3
U	32	67	125	34	34	24	64	0-4
V	33	70	126	17	17	25	65	0-5
W	34	71	127	31	31	26	66	0-6
X	35	72	130	27	27	27	67	0-7
Y	36	73	131	25	25	30	70	0-8
Z	37	74	132	21	21	31	71	0-9
Space	05	00	040	04	04	-	-	-
Tape Feed	-	-	-	-	00	-	-	-
Color Shift	-	-	-	-	02	-	-	-
Stop	-	-	-	-	43	-	-	-
Carriage Return	04	-	015	02	45	-	-	-
Shift Up	01	-	-	-	47	-	-	-
Shift Down	02	-	-	-	57	-	-	-
Tab	-	-	-	-	51	-	-	-
Backspace	-	-	-	-	61	-	-	-
Code Delete	-	-	-	-	77	-	-	-
Line Feed	03	-	012	10	-	-	-	-
Master Space	00	-	-	-	-	-	-	-
Figures	-	-	-	33	-	-	-	-
Letters	-	-	-	37	-	-	-	-

Character	1232 I/O Console Field Data	XS-3	ASCII	Teletype	Flexowriter UC	Flexowriter LC	BCD Tape Character	BCD Character	Card Punch
0	60	03	060	15	37		12	00	0
1	61	04	061	35	52		01	01	1
2	62	05	062	31	74		02	02	2
3	63	06	063	20	70		03	03	3
4	64	07	064	12	64		04	04	4
5	65	10	065	01	62		05	05	5
6	66	11	066	25	66		06	06	6
7	67	12	067	34	72		07	07	7
8	70	13	070	14	60		10	10	8
9	71	14	071	03	33		11	11	9
-	41	02	055	30	56	56	40	40	11
+	42	63	053	-	-	54	60	20	12
<	43	36	074	-	-		-	-	-
>	45	76	076	-	-		-	-	-
=	44	37	075	-	-	44	13	13	3-8
≠	-	60	-	-	-		-	-	-
−0	-	-	-	-	-		52	52	-
+0	-	-	-	-	-		72	32	-
)	40	77	051	11	42	-	74	34	12-4-8
(	51	55	050	36	46	-	34	74	0-4-8
.	75	22	056	07	-	42	73	33	-
/	74	64	057	27	54	-	21	61	0-1
\	-	15	134	-	-	-	-	-	-
:	55	43	041	26	-	-	-	-	-
"	52	-	042	21	-	-	-	-	-
:	53	21	072	16	-	-	-	-	-
·	-	-	-	-	44	-	-	-	12-3-8
,	56	62	54	06	-	46	33	73	0-3-8
;	73	16	073	17	-	-	-	-	-
1	-	-	-	-	-	50	-	-	-
—	46	-	-	-	50	-	-	-	-
#	50	41	052	-	-		-	-	11-4-8
$	47	42	044	22	-	53	53	53	11-3-8
@	-	56	100	-	-		-	-	-
'	72	40	047	32	-	14	14	-	-
#	-	35	043	-	-		-	-	-
&	-	20	046	13	-		-	-	-
?	54	23	077	23	-		-	-	-
←	-	-	137	-	-		-	-	-
↑	77	-	136	-	-		-	-	-
⊐	-	01	135	-	-		-	-	-
□	76	-	-	-	-		-	-	-
⊏	-	17	133	-	-		-	-	-
0	-	-	-	24	-		-	-	-
Δ	-	57	-	-	-		-	-	-
%	-	61	045	-	-		-	-	-

ASCII CODE

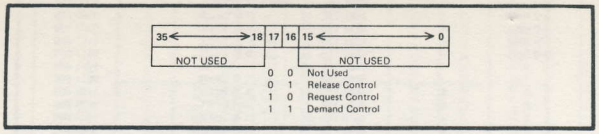
ASCII Code for the DEAC Keyboard Printer

Character Code Non-Print Codes	Printed Character	Functioning Keys	Character Code Printed Codes	Printed Character	Functioning Keys
000 0000		CTRL & @	010 1110	.	.
000 0001		CTRL & A	010 1111	/	/
000 0010		CTRL & B	011 0000	0	0
000 0011		CTRL & C	011 0001	1	1
000 0100		CTRL & EOT	011 0010	2	2
000 0101		CTRL & WRU	011 0011	3	3
000 0110		CTRL & RU	011 0100	4	4
000 0111		CTRL & BELL	011 0101	5	5
000 1000		CTRL & H	011 0110	6	6
000 1001		CTRL & I	011 0111	7	7
000 1010		Line Feed	011 1000	8	8
000 1011		CTRL & K	011 1001	9	9
000 1100		CTRL & L	011 1010	:	:
000 1101		Return	011 1011	;	;
000 1110		CTRL & N	011 1100	<	Shift & <
000 1111		CTRL & O	011 1101	=	Shift & =
001 0000		CTRL & P	011 1110	>	Shift & >
001 0001		CTRL & Q	011 1111	?	Shift & ?
001 0010		CTRL & Tape On	100 0000	@	Shift & @
001 0011		CTRL & X Off	100 0001	A	A
001 0100		CTRL & Tape Off	100 0010	B	B
001 0101		CTRL & U	100 0011	C	C
001 0110		CTRL & V	100 0100	D	D
001 0111		CTRL & W	100 0101	E	E
001 1000		CTRL & X	100 0110	F	F
001 1001		CTRL & Y	100 0111	G	G
001 1010		CTRL & Z	100 1000	H	H
001 1011		CTRL, Shift & K	100 1001	I	I
001 1100		CTRL, Shift & L	100 1010	J	J
001 1101		CTRL, Shift & M	100 1011	K	K
001 1110		CTRL, Shift & ↑	100 1100	L	L
001 1111		CTRL, Shift & ←	100 1101	M	M
111 1101		Alt. Mode	100 1110	N	N
111 1111		Rub Out	100 1111	O	O
			101 0000	P	P
Printed Codes			101 0001	Q	Q
			101 0010	R	R
010 0000	(space)	Space Bar	101 0011	S	S
010 0001	!	Shift & !	101 0100	T	T
010 0010	"	Shift & "	101 0101	U	U
010 0011	#	Shift & #	101 0110	V	V
010 0100	$	Shift & $	101 0111	W	W
010 0101	%	Shift & %	101 1000	X	X
010 0110	&	Shift & &	101 1001	Y	Y
010 0111	' (apos.)	Shift & '	101 1010	Z	Z
010 1000	(	Shift & (	101 1011	[	Shift & K
010 1001	)	Shift &)	101 1100	/	Shift & L
010 1010	*	Shift & *	101 1101	]	Shift & M
010 1011	+	Shift & +	101 1110	↑	Shift & ↑
010 1100	,	,	101 1111	←	Shift & ←
010 1101	-	-			

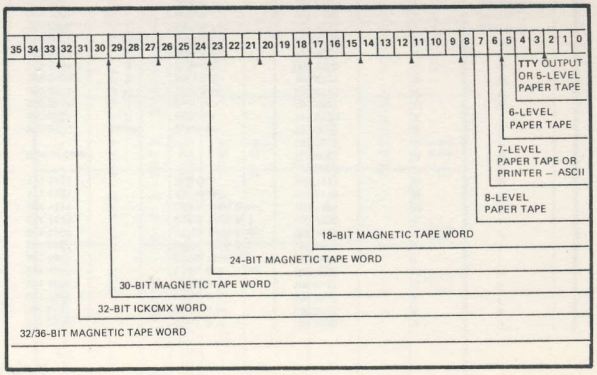
Note: CTRL is a key that deletes the 2^6 bit of the seven-bit code.

OJ-172(V) (DEAC)

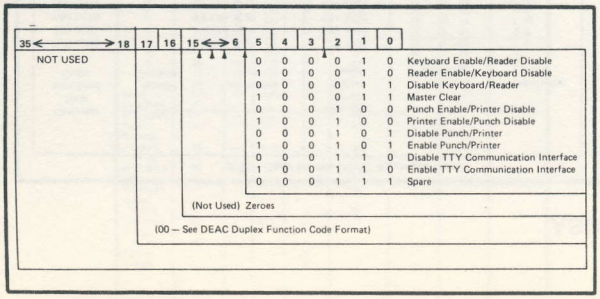
FUNCTION CODE FORMAT



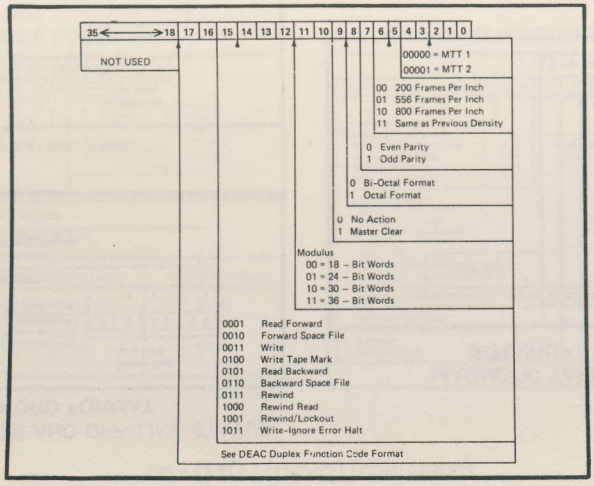
COMPUTER INPUT AND OUTPUT DATA WORD FORMAT



DEAC KEYBOARD, PRINTER, READER, PUNCH AND TTY FUNCTION CODE FORMAT

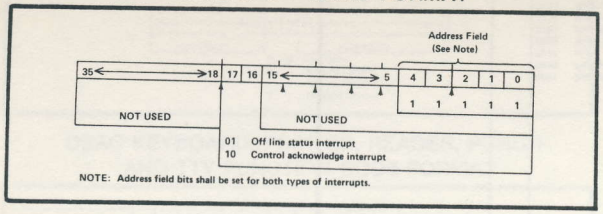


FUNCTION CODE FORMAT

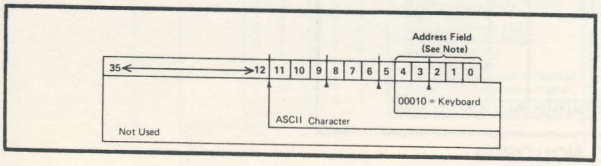


OJ-172(V) (DEAC) (continued)

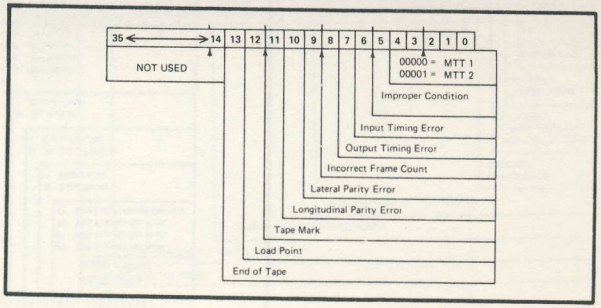
CONTROL ACKNOWLEDGE AND OFF-LINE STATUS INTERRUPT WORD FORMAT



KEYBOARD INTERRUPT WORD FORMAT

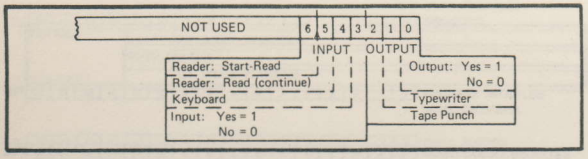


MAGNETIC TAPE TRANSPORT STATUS INTERRUPT WORD FORMAT



1232/1532 I/O CONSOLE

FUNCTION CODE FORMAT

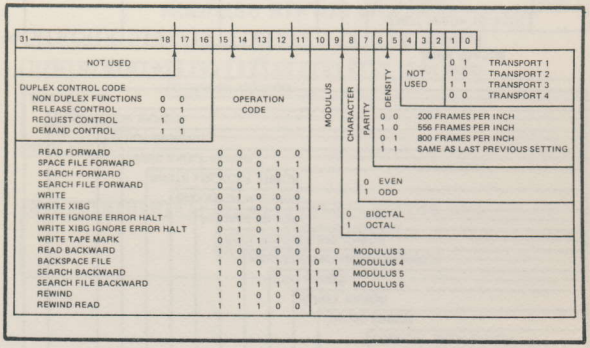


DATA FORMAT

EQUIPMENT	INTERFACE	KEYBOARD/PRINTER	READER/PUNCH
1232	8 Bit Maximum	Field Data Character (Modified)	Binary
1532	8 Bit Maximum	ASCII Character	Binary

AN/USH-19 MAGNETIC TAPE (7 TRACK)

FUNCTION WORD FORMAT



976X DISK WITH SI CONTROLLER

00_8 CONTROL REGISTER

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET+	OFFSET-	STROBE EARLY	STROBE LATE	*	FORMAT ENABLE	UNUSED						VERIFY	*	DONE	

* UNUSED

01_8 WORD COUNT REGISTER

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WORD COUNT															

02_8 PORT/CYLINDER ADDRESS REGISTER

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UNUSED			PORT SELECT			CYLINDER ADDRESS									

03_8 HEAD/SECTOR ADDRESS REGISTER

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UNUSED						HEAD ADDRESS				SECTOR ADDRESS					

05_8 ERROR REGISTER

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERROR FLAG	CONTENTION ERROR	SELECT ERROR	DRIVE FAULT ERROR	WRITE LOCKOUT ERROR	BAD SECTOR ERROR	FORMAT ERROR	SEEK INCOMPLETE ERROR	ADDRESS VERIFICATION ERROR	CRC ERROR	VERIFY ERROR	TIMING ERROR	OVERLAP SEEK ERROR	OVERLAP SEEK COMPLETE		

06_8 SEEK STATUS REGISTER

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PORT 1				PORT 2				PORT 3				SEEK COMPLETE	HARDWARE SEEK ERROR	BUSY ERROR	NOT READY TO SEEK

PORT 0

07_8 SEEK ADDRESS REGISTER

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UNUSED			PORT SELECT			CYLINDER ADDRESS									

10_8 DATA BUFFER

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA BUFFER															

11_8 COMMUNICATION REGISTER

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMMUNICATION REGISTER															

13_8 COMMAND REGISTER

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REGISTER ADDRESS INCREMENT				READ WRITE	OPERATION SELECT	REGISTER WORD COUNT				REGISTER ADDRESS					

ADDRESS STATUS WORDS

1ST WORD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WRITE PROTECT	BAD SECTOR					CYLINDER NUMBER									

2ND WORD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							HEAD NUMBER				SECTOR NUMBER				

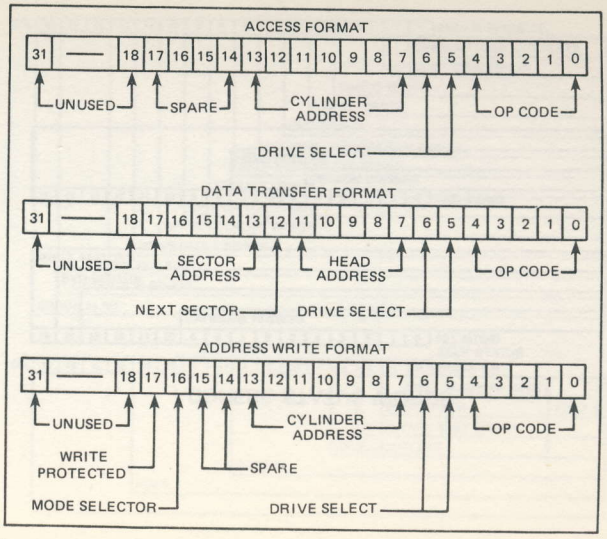
RD-281(V), (V)1, (V)2, (V)3 DISK

OP CODE ASSIGNMENTS

Instruction	Op Code Bits 4	3	2	1	0
Access					
Direct Seek	0	0	0	0	1
Master Clear	0	0	0	1	0
Data Transfer					
Write Track	0	0	1	0	0
Write Sector	1	0	1	0	1
Write Track Cylinder	1	0	1	1	0
Write Sector Cylinder	0	0	1	1	1
Read Track	0	1	0	0	0
Read Sector	1	1	0	0	1
Read Track Cylinder	1	1	0	1	0
Read Sector Cylinder	0	1	0	1	1
Address Write					
Write Address	1	0	0	1	1
DSU Status Request					
Status Request	1	0	0	0	0
DSU Initialization					
No Op*	1	1	1	1	1
Spare	1	1	1	0	0
Spare	0	1	1	0	1
Spare	0	1	1	1	0

*Used to transmit duplexer instruction in vertical model.

INSTRUCTION WORD FORMATS



FILE-GENERATED INTERRUPT WORD

RD-281(V), (V)1, (V)2 Bit No.	Status Definition	RD-281(V)3 Bit No.	Status Definition
17	Seek Complete, Lower Bank	17	Seek Complete, Drive 3
16	Seek Complete, Upper Bank	16	Seek Complete, Drive 2
15		15	Seek Complete, Drive 1
14		14	Seek Complete, Drive 0
13	Selected Head Address	13	
12		12	
11		11	Selected Head Address
10	Cylinder-Counter Busy	10	
9	Drive Inoperative	9	
8	Illegal Message Length	8	Drive Inoperative[2,3]
7	Illegal Instruction	7	Invalid Data[3]
6	Read/Write Complete	6	Read/Write Complete
5	File Generated Interrupt Word[4]	5	File Generated Interrupt Word[4]
4	Over Temperature	4	Illegal Instruction
3	EMI	3	Over Temperature
2	Address No Compare[1]	2	EMI
1	Unsafe	1	Address No Compare[2]
0	Invalid Data	0	Unsafe

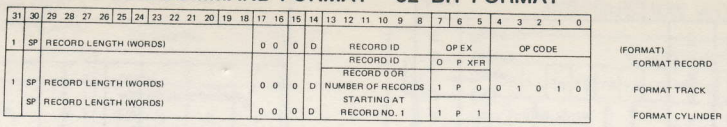
Notes:
[1]Bit 9 plus bit 2 = Sector Counter Error.
[2]Bit 8 plus 1 = Sector Counter Error.
[3]Bit 8 plus bit 7 = Illegal Message Length.
[4]When Bit 5 is logical "1," indicates the interrupt was generated by the AN/UYH-2(V)

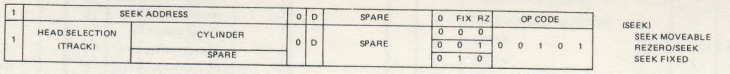
COMPUTER-REQUESTED INTERRUPT WORD

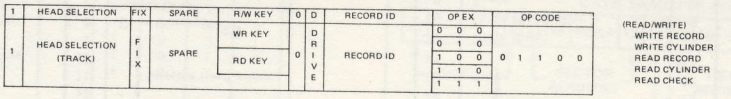
RD-281(V), (V)1, (V)2 Bit No.	Status Definition	RD-281(V)3 Bit No.	Status Definition
17		17	Drive Busy
16		16	
15		15	
14	Cylinder Address of Selected Drive	14	
13		13	Cylinder Address of Selected Drive
12		12	
11		11	
10	Drive Busy	10	
9	Drive Inoperative	9	
8	Spare	8	Drive Inoperative
7	Spare	7	Spare
6	Spare	6	Spare
5	Computer Requested Interrupt Word[1]	5	Computer Requested Interrupt Word[1]
4	Over Temperature	4	Spare
3	EMI	3	Over Temperature
2	Spare	2	EMI
1	Unsafe	1	Spare
0	Spare	0	Unsafe

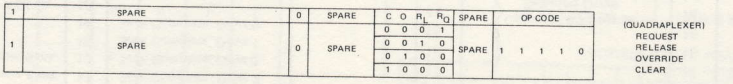
Note:
[1]When Bit 5 is a logical "0," indicates the interrupt was requested by the data processor.

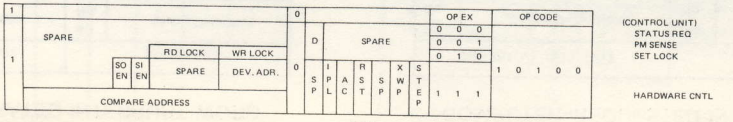
DMS MODE COMMAND FORMAT – 32-BIT FORMAT











DMS MODE INTERRUPT WORD

Bit No.	Title	Definition
(0)	Read Error	Error in reading data module (per error detection code process).
(1)	DMS Fault	Fault in drive, adapter, or processor (Issue PM Sense EF for detailed status).
(2)	ID Error	ID not found.
(3)	Command Range Reject	Out of bounds argument with command.
(4)	Over Temperature	Temperature beyond tolerable thresholds.
(5)	Status/PM Sense	Host requested status or PM Sense complete.
(6)	R/W Complete	The read or write operation was completed.
(7)	Command Reject	Illegal command, or legal but cannot honor at this time for reasons given. Bit(s) 1, 2, 3, 9, 11, 13, 16, 18 also set.
(8)	Data Overrun	Attempt to write more data than available in a record, a track or a cylinder.
(9)	DDU Not Ready	DDU is not loaded, up to speed, at home or where last commanded.
(10)	Lock Set	The Read/Write Lock has been accepted and stored.
(11)	Protected Record	Attempt to read or write a protected record, Read Key/Read Lock or Write Key/Write Lock mismatch detected.
(12)	Data Underrun	Channel did not provide or take the number of words specified or available in the record.
(13)	Seek Error	Verify process reveals that the AN/UYH-2(V) did not acquire the cylinder and/or head specified.
(14)	Overridden	Indicates loss of control of the AN/UYH-2(V) by an Override command from another channel.
(15)	Low 16	Always a logical 0 to indicate the low order 16 bits of the DMS interrupt word.
(16)	Format Overrun	Attempt to format track beyond capacity.
(17)	Seek Acknowledged	Acknowledges receipt of seek commands, addresses cylinder and head stored for subsequent use.
(18)	Power Fault	Power supply voltages outside of allowable tolerance.
(19)	Control Acquired	Host has acquired control of the AN/UYH-2(V)
(20)	Control Released	Host has released control of the AN/UYH-2(V)
(21-28)	Spare	
(29)	Drive Selection	Indicates the selected drive (DMS+1 only)
(30)	Spare	Power supply voltage outside of allowable tolerance.
(31)	High 16	Always a logical 1 to indicate the high order 16-bits of the DMS interrupt word.

COMMAND OPERATION CODES

COMMAND	BITS 15	14	13	12	CLASS
STATUS REQUEST	0	0	0	0	ACCESS
DIRECT SEEK	0	0	0	1	ACCESS
RETURN SEEK	0	0	1	0	ACCESS
MASTER CLEAR	0	0	1	1	ACCESS
FORMAT	0	1	0	0	ACCESS
MODE CHANGE	0	1	0	1	ACCESS
OFFSET STROBE ERROR RECOVERY	0	1	1	0	OFFSET/STROBE
WRITE ADDRESS	0	1	1	1	WRITE ADDRESS
INPUT DATA	1	0	0	0	DATA TRANSFER
OUTPUT DATA	1	0	0	1	DATA TRANSFER
VERIFY CHECKWORD	1	0	1	0	DATA TRANSFER
DIAGNOSTIC TEST	1	0	1	1	DIAGNOSTIC
SET SECTOR SIZE	1	1	0	0	SECTOR SIZE
(ILLEGAL)	1	1	0	1	
(ILLEGAL)	1	1	1	0	
NO OPERATION	1	1	1	1	ACCESS

INTERRUPT WORD ASSIGNMENTS

NTDS Bit	Description
15	SEEK ERROR
14	POWER FAILURE
13	BAD SECTOR/NO ROOM
12	DIAGNOSTIC TEST FAILURE
11	OPERATION COMPLETE
10	LOST DATA
09	ILLEGAL INSTRUCTION
08	ADDRESS CHECKWORD OR DATA FIELD CHECKWORD ERROR
07	ADDRESS ERROR OR ADDRESS CHECKWORD ERROR
06	LOST SECTOR
05	WRITE PROTECT VIOLATION
04	CHECK DIAGNOSTIC
03	NO RESPONSE
02	PARITY ERROR
1-0	LOGICAL UNIT NUMBER

STATUS WORD FORMAT

NTDS Bit		Description
WORD 1	14-15	ZERO (SPARES)
	13	ON CYLINDER
	12	UNIT READY
	11	ONE
	10	ZERO
	9	OFFSET ACTIVE
	8	ATTENTION
	7	NO HEAD SELECT
	6	WRITE FAULT
	5	(W+R) OFF CYLINDER
	4	W R FAULT
	3	VOLTAGE FAULT
	2	HEAD SELECT FAULT
	1	SEEK ERROR
	0	WRITE PROTECT
WORD 2	15	EARLY STROBE
	14	LATE STROBE
	13	POSITIVE OFFSET
	12	NEGATIVE OFFSET
	10-11	ZERO (SPARES)
	0-9	CYLINDER NUMBER
WORD 3	11-15	HEAD NUMBER
	6-10	LAST SECTOR
	0-5	ZERO (SPARES)
WORD 4	0-15	ZERO (SPARES)

AN/UYH-3(V) COMMAND WORD FORMATS

ACCESS CLASS

15 12	11 10	9 0
OP CODE	UNIT*	CYLINDER NUMBER**

WRITE ADDRESS CLASS/FIRST WORD

15 12	11 10	9 0
OP CODE	UNIT	

WRITE ADDRESS CLASS/SECOND WORD

15 14	13 12	11	10	9 5	4 0
	AMOUNT TO WRITE	BAD SEC	WRT PRT	HEAD NUMBER	SECTOR NUMBER

OFFSET/STROBE CLASS

15 12	11 8	7	6	5	4	3 0
OP CODE		EARLY STROBE	LATE STROBE	POS. OFFSET	NEG. OFFSET	

SECTOR SIZE CLASS/FIRST WORD

15 12	11 10	9 6	5 0
OP CODE	UNIT		NUMBER OF SECTORS/TRACK

SECTOR SIZE CLASS/SECOND WORD

15 12	11 0
	NUMBER OF WORDS PER SECTOR

DATA TRANSFER CLASS/FIRST WORD

15 12	11 10	9 5	4 0
OP CODE	UNIT	HEAD NUMBER	SECTOR NUMBER

DATA TRANSFER CLASS/SECOND WORD

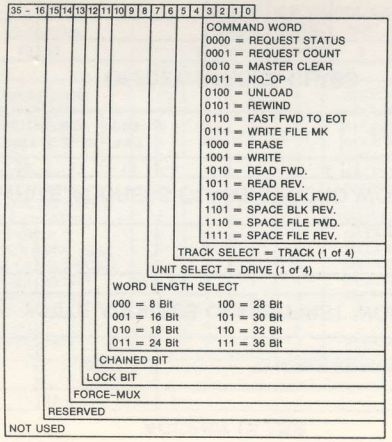
15 0
NUMBER OF WORDS -1

* This field is not used for a master clear or operating mode change command.

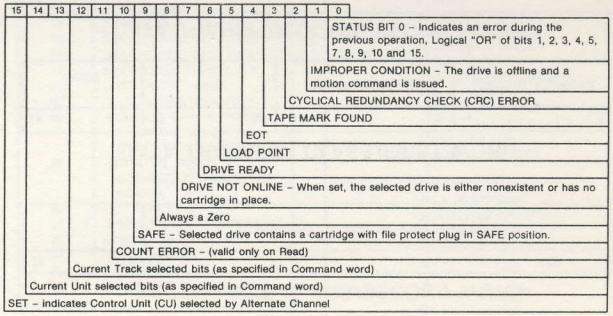
** This field is not used for a status request, master clear, or operating mode change command.

QANTEX CMTU AN/USH-26(V)

CONTROL WORD FORMAT



STATUS WORD



AN/UYK–7(V) MISC DATA

APPROXIMATE POWER CONSUMPTION/HEAT DISSIPATION

Modules	Power	Heat
Input/Output Adapter	205 Watts	700 BTU/hr
Input/Output Controller	440 Watts	1504 BTU/hr
Central Processor Unit	504 Watts	1730 BTU/hr
Core Memory Unit	210 Watts	715 BTU/hr
Double–Density Film Memory Unit	250 Watts	853 BTU/hr
Power Supply	360 Watts	1230 BTU/hr
Cabinet	150 Watts	510 BTU/hr
Test Set/Maintenance Panel	15 Watts	51 BTU/hr

APPROXIMATE WEIGHTS

Modules	Approximate Weight in Lbs.
Input/Output Adapter Unit	52
Input/Output Controller Unit	48.5
Central Processor Unit	49
Core Memory Unit	47.5
Double–Density Film Memory Unit	52
Power Supply Unit	65
Dummy Adapter Unit	12
Dummy Memory Chassis	6
Single–Bay Cabinet	190

ABBREVIATED OPERATING INSTRUCTIONS FOR AN/UYK-7(V) COMPUTER DIAGNOSTICS
(Refer to NAVSEA 0967-024-5454 Parts 1, 2, 3, 4)

BOOTSTRAP LOAD
1. Set Bootstrap switches to proper position
2. Set A3 to Load Channel
3. Set S1 to Load Bias
4. Set S6 to Load Bias + 37700

CPU DIAGNOSTIC OPERATING PROCEDURES (2 seconds)
1. Set P to 0 + S1
2. Set S1 to Load Bias
3. Set A0 to IOC Number Octal

IOC/IOA DIAGNOSTIC (25 seconds)
1. Set P to 0 + S3
2. Set S3 to 20000 + Load Bias
3. Set A0 to IOC Number Octal
4. Set A1 to Channels to Test (Bit Position)
5. Set A2 to Intercomputer Channels to Test
6. Set A3 to End-Around-Channels

MEMORY DIAGNOSTIC (25 seconds)
1. Set P to 0 + S2
2. Set S2 to 30000 + Load Bias
3. Set A0 to IOC Number Octal
4. Set A6 to Memory Banks to test
5. Set A7 to Memory Options
   - Bit 31 to bypass I Bus Test
   - Bit 30 to bypass Pattern Test
   - Bit 16 to Select DDFM Disturb Test

KEY OPTIONS

JUMP 1	=	Interleaved Core Memory
JUMP 2	=	End-Around-Channels
JUMP 3	=	Loop on Diagnostic
STOP 4	=	Unexpected Class I Interrupt
STOP 5	=	Error Stop
STOP 6	=	End of Individual Diagnostic test
STOP 7	=	End of Individual Subtest

CONFIDENCE TEST
1. Set P to S1 + 17770
2. Set S1 to Load Bias
3. Set A0 to IOC Number Octal
4. Set A1 to Channels to test (bit position)
5. Set A2 to Intercomputer Channels to test
6. Set A3 to End-Around-Channels
7. Set A6 to Banks to Test
8. Set A7 to Memory Options
   - Bit 31 to bypass I Bus Test
   - Bit 30 to bypass Pattern Test
   - Bit 16 to Select DDFM Disturb Test

(For Supplementary Diagnostic Tests see Diagnostic Operating Procedures Manual).

AN/UYK-7(V) PUBLICATIONS/HARDWARE

Document No.	Description
A962	Log, Operation and Maintenance
UD1-3748	Report, Equipment Malfunction
UD1-3650	Report, AN/UYK-7(V) Warranty
SE610-AW-MMA-010	Maintenance Manual, Vol. 1 for Computer Set AN/UYK-7(V), Chapters 1-3
SE610-AW-MMA-020	Maintenance Manual, Vol. 2 for Computer Set AN/UYK-7(V), Chapters 4-8
SE610-AW-MMA-030	Maintenance Manual, Vol. 3 for Computer Set AN/UYK-7(V), Circuit Diagrams, Part 1
SE610-AW-MMA-040	Maintenance Manual, Vol. 3 for Computer Set AN/UYK-7(V), Circuit Diagrams, Part 2
NAVSEA 0967-LP-024-5454	Diagnostic Operating Procedures, Parts 1-4
NAVSEA 0967-LP-024-5464	Diagnostic Program Listing, Parts 1 and 3
NAVSEA 0967-LP-024-5474	Paper Tape, CPU, IOC & Memory Diagnostic Test Program, Part I (KA-S000029-000-01) Supplementary Diagnostic Test Program, Part II, Paper Tape (KA-S000030-000-01) CPU, IOC and Memory Diagnostic Programs, Part III, Magnetic Tape (GA-S000031-000-01) Supplementary Diagnostic Test Programs, Part IV, Magnetic Tape (GA-S000032-000-01)
NAVSEA 0967-LP-024-5780	NDRO Operating Procedures Manual

Field Change Documentation Packages
AN/UYK-7(V) Configuration Data Summary
AN/UYK-7(V) Computer Set, Configuration Item Index, Site Version

Hardware	
7073330-XX TS-2940V/UYK-7(V)	Test Set (Maintenance Panel)
7071687-XX C-8542/UYK-7(V)	Remote Operator's Control Unit
7151579-00	Card Puller, Double Width
7151580-00	Card Puller, Single Width
7151615-01	Torque Wrench, Heat Exchanger Bolts

FIELD CHANGE/ECP EFFECTIVITY

System			
FC	ECP	FC	ECP

Cabinet			
FC	ECP	FC	ECP
1	205	3	344*
2	275	4	348*

Maintenance Console			
FC	ECP	FC	ECP
1	275		

Remote Console			
FC	ECP	FC	ECP
1	348*		

PS 208V			
FC	ECP	FC	ECP
1	246	8	335*
2	221		
3	196		
4	241		
5	302		
6	305		
7	332		
7	334		

CPU			
FC	ECP	FC	ECP
1	228		
1	229		
2	236		
3	247		
4	290		
5	241		
6	313		
7	306		
7	316		
8	329		
8	331		
9	391*		

CMU			
FC	ECP	FC	ECP
1	277		
2	236		
3	286		
4	196		
5	287		
6	287		
7	304		
8	313		
9	353		

DDMFM			
FC	ECP	FC	ECP
1	295		
2	196		
3	300		
4	313		
5	311		
5	322		
6	326		
7	328		
8	383		
9	372*		
10	404*		

IOC			
FC	ECP	FC	ECP
1	237		
2	236		
3	241		
4	272		
4	294		
5	313		
6	292		
7	351		
8	373*		
9	398		

IOA			
FC	ECP	FC	ECP
1	227		
2	236		
3	286		
4	241		
5	313		
6	366*		

PS 115V			
FC	ECP	FC	ECP
1	246	8	335*
2	221		
3	196		
4	241		
5	302		
6	305		
7	332		
7	334		

*NOTE: Limited retrofit. Not available to all users.

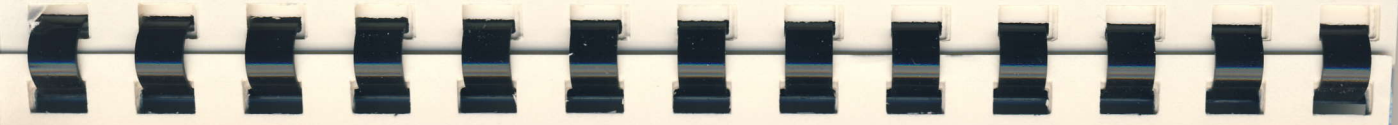
NOMENCLATURED ITEMS

Unit Name	Designation	Sperry Part Number
CABINET, ELECTRICAL EQUIPMENT	CY-6797/UYK-7(V)	7073260
CABINET, ELECTRICAL EQUIPMENT	CY-6798/UYK-7(V)	7073260
CABINET, ELECTRICAL EQUIPMENT	CY-6799/UYK-7(V)	7073260
CABINET, ELECTRICAL EQUIPMENT	CY-6800/UYK-7(V)	7073260
CABINET, ELECTRICAL EQUIPMENT	CY-6721/UYK-7(V)	7073260
CABINET, ELECTRICAL EQUIPMENT	CY-7196/UYK-7(V)	7073260
CABINET, ELECTRICAL EQUIPMENT	CY-7197/UYK-7(V)	7073260
CABINET, ELECTRICAL EQUIPMENT	CY-7198/UYK-7(V)	7073260
POWER SUPPLY	PP-6395/UYK-7(V)	7073375
POWER SUPPLY	PP-6258/UYK	7071630
CONTROLLER UNIT, INPUT-OUTPUT	C-8408(P)/UYK-7(V)	7073320
CENTRAL PROCESSOR UNIT	CP-1036(P)/UYK-7(V)	7073540
CORE MEMORY UNIT	MU-558/UYK	7071520
FILM MEMORY UNIT	MU-642/UYK-7(V)	7126526
ADAPTER UNIT, INPUT-OUTPUT	MX-8450(P)/UYK	7071570
ADAPTER UNIT, INPUT-OUTPUT	MX-8537(P)/UYK-7(V)	7073400
INTERFACE KIT, SERIAL	MK-1731/UYK-7(V)	7073304
INTERFACE KIT, SLOW	MK-1732/UYK-7(V)	7073302
INTERFACE KIT, FAST, NEGATIVE	MK-1733/UYK-7(V)	7073301
INTERFACE KIT, FAST, POSITIVE	MK-1734/UYK-7(V)	7073303
CONTROL, COMPUTER	C-8542/UYK-7(V)	7071687
TEST SET, COMPUTER LOGIC UNIT	TS-2940(V)/UYK-7(V)	7073330
WATER COOLING KIT, ONE BAY	MK-2248(V)/UYK-7(V)	7322851
WATER COOLING KIT, TWO BAY	MK-2249(V)/UYK-7(V)	7322852
WATER COOLING KIT, THREE BAY	MK-2250(V)/UYK-7(V)	7322853
WATER COOLING KIT, FOUR BAY	MK-2251(V)/UYK-7(V)	7322854

LINE REPLACEABLE ASSEMBLIES

Sperry Part Number	Description	National Stock Number
7056763-02	CCA OSCILLATOR	5999-01-067-8153
7071530-03	MEMORY STACK ASSY 4K, 32 BIT	7025-01-065-8209
7071720-11	SWITCHING REGULATOR ASSY	7050-01-101-5849
7071866-01	CCA WIRED-DELAY LINE CLOCK	5999-01-067-8154
7071867-01	CCA WIRED-DELAY LINE CLOCK	7025-01-065-8667
7073075-11	REGULATOR OSCILLATOR UNIT 20 VDC	7025-01-086-3001
7073175-10	REGLTR CONV ASSY POWER SUPPLY	6130-01-067-3274
7093362-01	MEM STACK MDL 16K DD, MATED FILM	7025-01-063-6939
7093385-06	CCA SENSE DIGIT	5999-01-089-1466
7093390-01	CCA LOWER DIVERTER	7025-01-068-4814
7093395-01	CCA UPPER DIVERTER	7025-01-069-2436
7093405-01	CCA WRITE CONTROL	7025-01-065-8659
7093410-01	CCA CHANNEL ADD REGISTER CONTROL	7025-01-067-3706
7093415-01	CCA TEMP SENSOR, REAR	7025-01-067-3707
7093420-01	CCA TEMP SENSOR, FRONT	7025-01-067-3702
7093425-01	CCA UPPER DIVERTER TRANSLATION	7025-01-067-3703
7093430-05	CCA LINE CHARGER	7025-01-067-3725
7093435-06	CCA WORD CURRENT GENERATOR	5999-01-078-7057
7093440-01	CCA TIMING FLIP-FLOP	7025-01-067-3727
7093445-01	CCA STROBE DELAY LINE	7025-01-067-3722
7093470-01	CCA UPPER CHANNEL ACTIVE	7025-01-067-0755
7093475-01	CCA LOWER CHANNEL ACTIVE	7025-01-067-0756
7093485-01	CCA BYTE CONTROL	7025-01-067-3714
7093491-01	CCA DATA STORAGE	7025-01-067-3715
7093495-01	CCA ADDRESS STORAGE	7025-01-067-3708
7111005-02	CCA 1 SHOTS, SYNC AND DATA REGISTERS	5895-00-760-6927
7111400-01	CCA READ/WRITE DIODE SELECTOR	7025-01-066-7422
7111405-02	CCA READ/WRITE SECONDARY SELECTOR	7025-01-066-7416
7111436-01	CCA SENSE AMPLIFIER	7025-01-067-0743

Sperry Part Number	Description	National Stock Number
7111755-02	CCA CONTROL TYPE 4	7025-01-065-5770
7111877-02	CCA CONSOLE CONTROL	7025-01-066-7423
7111886-02	CCA F TRANSLATOR III	7025-01-065-4689
7111890-02	CCA F TRANSLATOR IV	5999-01-098-6592
7111895-02	CCA F TRANSLATOR I	7025-01-065-4690
7111905-04	CCA CONTROL MEMORY	7025-01-065-4691
7111910-02	CCA DIR REGISTER X8	7025-01-065-4692
7111915-02	CCA CHAIN ACTIVE X8	7010-01-100-6849
7111920-02	CCA CHANNEL AND MONITOR ACTIVE	7025-01-065-5638
7111926-02	CCA CIR REGISTER	7025-01-065-4693
7111931-02	CCA INTERCOMPUTER LOGIC CHANNEL	7025-01-065-4694
7111937-02	CCA INTERCOMPUTER LOGIC GROUP	7025-01-065-4695
7111940-02	CCA CONTROL MEMORY ADDRESS REGISTER	7025-01-065-4696
7111945-02	CCA CONTROL LOGIC	7025-01-065-4697
7111955-02	CCA V TRANSLATOR I	5999-01-064-0748
7111965-02	CCA F TRANSLATOR V	5999-01-064-0754
7111970-02	CCA F TRANSLATOR VI	5999-01-064-0755
7111981-02	CCA ACCUMULATOR AND C SELECTOR	5999-01-075-6049
7111987-02	CCA U REGISTER	5999-01-064-0757
7112010-02	CCA D AND Q REGISTER	7025-01-065-4698
7112015-02	CCA X REG, X, D AND Q SEL	7025-01-065-5704
7112025-02	CCA K AND K REGISTER	5999-01-064-0758
7112036-02	CCA V, F, PARITY	5999-01-064-0759
7112040-02	CCA SHIFT CONTROL I	5999-01-064-0767
7112045-02	CCA SHIFT CONTROL II	5999-01-064-0768
7112050-02	CCA MAIN TIMING CONS SEL	5999-01-064-0769
7112055-02	CCA A CONTROL I	5999-01-064-0770
7112061-02	CCA A CONTROL II	5999-01-064-0771
7112065-02	CCA A CONTROL III	7025-01-065-8623



7111440-03	CCA X-Y READ/WRITE CURRENT REGULATOR	7025-01-067-0750
7111446-02	CCA ARITH DETECTION CKTS I	7025-01-067-0744
7111451-02	CCA ARITH DETECTION CKTS II	7025-01-065-5773
7111465-01	CCA INTERFACE CONTROL	7025-01-066-8141
7111470-01	CCA PRIORITY EVALUATION	7025-01-065-8628
7111476-02	CCA ARITH DETECTION CKTS III	7025-01-065-8629
7111482-02	CCA ARITH DETECTION CKTS IV	7025-01-065-8630
7111485-04	CCA THERMOSTAT, REAR	7025-01-065-8641
7111490-04	CCA THERMOSTAT, FRONT	7025-01-065-8642
7111505-02	CCA AMP LINE DRIVER -3V INTERFACE	7025-01-065-8643
7111511-03	CCA ACKNOWLEDGE TIMING CARD 1 FAST	7025-01-065-5700
7111517-03	CCA AMPLIFIER INPUT -3V INTERFACE	7025-01-066-8142
7111520-03	CCA AMPL, LINE DRIVER -15V INTERFACE	7025-01-076-0592
7111527-03	CCA ACKNOWLEDGE TIMING CARD 1 SLOW	7025-01-065-8622
7111530-01	CCA AMPLIFIER INPUT -15V INTERFACE	7025-01-065-8685
7111535-02	CCA ACKNOWLEDGE TIMING CARD 2 SLOW	7025-01-065-8686
7111540-02	CCA ACKNOWLEDGE TIMING CARD 2 FAST	7025-01-065-8687
7111545-04	CCA INTEGRATED REGISTER ARRAY	7025-01-065-8676
7111560-02	CCA MAIN MEMORY ADDRESS REGISTER	7025-01-065-8688
7111581-02	CCA CHANNEL PRIORITY	7025-01-065-8677
7111605-02	CCA F TRANSLATOR II	7025-01-065-8651
7111610-02	CCA OCTAL TRANSLATOR	7025-01-065-8652
7111615-02	CCA INHIBIT CURRENT REGULATOR	5999-00-494-8045
7111620-05	CCA INHIBIT STACK SELECTOR	7025-01-065-8644
7111635-02	CCA SHIFT NETWORK	7025-01-065-5701
7111655-04	CCA SUBCONTRACTOR	7025-01-065-5702
7111655-01	CCA RESISTOR NETWORK	7025-01-067-3729
7111675-02	CCA SHIFT COUNT REGISTER	7025-01-065-5703
7111692-02	CCA MEMORY CONTROL	7025-01-065-5767
7111701-01	CCA VOLTAGE SENSOR	5999-01-075-6050
7111705-02	CCA MASTER CLEAR DRIVER	7025-01-065-5768
7111750-02	CCA CONTROL TYPE 3	7025-01-065-5769

7112077-02	CCA X, MULT CONTROL	5999-01-075-6048
7112081-02	CCA SS, XS CONTROL	5999-01-101-4467
7112085-02	CCA INT CODE FORMATION	7025-01-066-2218
7112090-02	CCA D, Q, CONTROL	7025-01-066-7401
7112096-02	CCA DS, QS, WS, AND ZS CONTROL	7025-01-066-2219
7112101-02	CCA M, QS CONTROL	7025-01-066-2235
7112106-02	CCA W AND Z CONTROL	7025-01-066-2236
7112112-02	CCA IOC INT AND INT SUB SEQ	7025-01-066-2237
7112130-00	CCA ISOLATE	5999-00-464-6308
7112135-00	CCA R.C. NETWORK	5999-00-464-6352
7112140-00	CCA R.C. NETWORK-EXT	5999-00-464-6362
7112290-02	CCA SINGLE INVERTERS	7025-01-066-2238
7112298-02	CCA INT CONTROL IV	7025-01-065-4699
7112310-02	CCA V SEL, K XLTR, Q REG CONT	7025-01-065-4700
7112315-02	CCA F TRANSLATOR VII	7025-01-065-4701
7112320-02	CCA SHIFT ENABLE AND SCR SELECT	7025-01-065-4702
7112331-02	CCA ARITH CLOCK CONTROL	7025-01-065-4703
7112335-02	CCA GENERATOR 2 INPUT	7025-01-065-5663
7112365-02	CCA CURRENT SWITCH	5895-00-585-0083
7112370-02	CCA SELECTION MATRIX	7025-01-065-5664
7112820-02	CCA P REG, R REG	7025-01-065-5665
7112825-02	CCA BP, Y, P*ST REG	7025-01-065-5672
7112830-02	CCA G CM, MLO CHECK H REG	7025-01-065-4704
7112835-02	CCA S CM AND BASE ADDER	7025-01-065-4705
7112840-02	CCA B + Y ADDER, U SEL	7025-01-065-4706
7112845-02	CCA CM SELECT	7025-01-065-4707
7112850-02	CCA SEQUENCE AND ROM ADD SEL	7025-01-065-4708
7112855-02	CCA S, G, CM SEL AND G CM	7025-01-065-4709
7112860-02	CCA Y + B ADDER PS, RS HS REG	7025-01-065-4710
7112865-02	CCA U, P + S ADDER CONTROL I	7025-01-065-4711
7112870-02	CCA B SEL AND PS CM	7025-01-065-4712
7112876-02	CCA C RG CONTROL I	7025-01-065-4713

CCA = Circuit Card Assembly

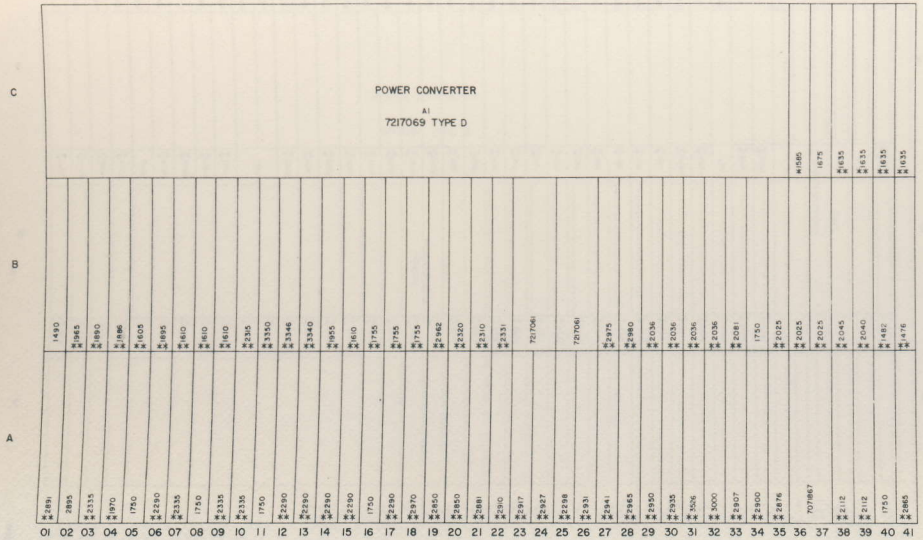
LINE REPLACEABLE ASSEMBLIES (continued)

Sperry Part Number	Description	National Stock Number
7112881-01	CCA TIMEOUT, MON CLK, ROM CONTROL	5999-01-098-6593
7112891-02	CCA U TRANSLATION I	7025-01-065-4715
7112895-02	CCA U TRANSLATION II	7025-01-065-4716
7112900-02	CCA SA AND OP REQ ENABLE	7025-01-065-4717
7112907-02	CCA SEQ HOLD	7010-01-100-6850
7112910-02	CCA BP MLO ERRORS	5999-01-098-6594
7112917-02	CCA CLR STATUS AND REI	7025-01-065-4718
7112920-03	CCA M REGISTER AND O BUSS	5999-01-132-4165
7112927-02	CCA INT REG AND STAT REG	7025-01-064-0798
7112931-02	CCA MOL AND ROM START	7025-01-064-0781
7112935-02	CCA ARITH CM COMMANDS	7025-01-064-0782
7112941-02	CCA MEMORY ENABLE	7025-01-064-0783
7112945-03	CCA M REG WRITE BYTE II	7025-01-080-4663
7112950-02	CCA ARITH CONTROL COMMANDS	7025-01-064-0790
7112962-02	CCA EARLY HOLD CONTROL	7025-01-064-0791
7112965-02	CCA MISC REG COMMANDS I	7025-01-064-0792
7112970-02	CCA MISC TRANSLATION I	7025-01-064-0793
7112975-02	CCA ARITH COMMANDS I	7025-01-064-0799
7112980-02	CCA ARITH COMMANDS II	7025-01-064-0800
7112985-02	CCA INT ATO AND ACC GATES	5999-01-064-0772
7113000-02	CCA RPT, REG CONTROL II	5999-01-064-0784
7113021-01	CCA SHIFT REGISTER	5999-01-064-0785
7113026-01	CCA INPUT CONTROL	5999-01-065-4720
7113031-01	CCA FUNCTION REGISTER	5999-01-065-4721
7113036-01	CCA MODE CONTROL	5999-01-065-4722
7113040-01	CCA TIME DELAY	5999-01-065-4723
7113051-01	CCA DELAY LINE AND CLOCK	5999-01-065-4724
7113056-01	CCA TRANSCEIVER	5999-01-065-4725
7113061-01	CCA DEMODULATOR	7025-01-065-5661

CCA = Circuit Card Assembly

Sperry Part Number	Description	National Stock Number
7113330-02	CCA AMP LINE DRIVER +3V	7025-01-065-5673
7113336-02	CCA AMPLIFIER INPUT +3V	7025-01-072-2456
7113340-02	CCA V TRANSLATION II	7025-01-065-5676
7113346-02	CCA V TRANSLATION III	7025-01-065-5683
7113350-02	CCA V TRANSLATION IV	7025-01-065-5690
7113386-01	CCA CLOCK SELECTOR AND DEMODULATOR	7025-01-064-0801
7113390-00	CCA DELAY LINE DEMODULATOR	5999-01-023-8478
7113395-00	CCA DELAY	5999-01-023-9412
7113410-01	CCA NETWORK LOGIC INVERTER	7025-01-064-0802
7113516-01	CCA CLOCK CONTROL AND COUNTER	7025-01-064-0803
7113526-02	CCA U/L, CONS AND U REG CONT	7025-01-064-0804
7129550-01	CONVERTER MODULE ASSY	7025-01-065-4688
7139190-02	CCA Z AND S REGISTERS	7025-01-112-1385
7151585-02	CCA VOLTAGE SENSOR	7025-01-065-4728
7165475-01	CCA PRIORITY PROCESSING	7025-01-095-4932
7165530-01	CCA MAIN DELAY LINE 1	5999-01-101-4469
7165534-02	CCA MEMORY TIMING	5999-01-117-5734
7165535-01	CCA MAIN DELAY LINE 2	5999-01-096-6632
7165540-01	CCA MAIN DELAY LINE 3	7025-01-093-6198
7165546-01	CCA MAIN DELAY LINE 4	5999-01-145-6569
7165551-00	CCA TRANS AND PRIMARY SEL	5962-01-121-2987
7165553-00	CCA TRANS AND PRIMARY SEL	5962-01-101-6408
7216492-06	RESISTOR MODULE ASSY	7010-00-283-2160
7216965-01	CCA DELAY LINE CLOCK	7025-01-065-4604
7217061-01	CCA DELAY LINE CLOCK	7025-01-065-4605
7217069-01	CONVERTER MODULE ASSY	7050-01-065-4686
7217072-02	CONVERTER MODULE ASSY	7050-01-070-0358
7217074-02	CONVERTER MODULE ASSY	7050-01-065-4687
7217225-00	CCA TERMINAL	7010-01-116-7742

CENTRAL PROCESSOR CARD PLACEMENT, PART 1



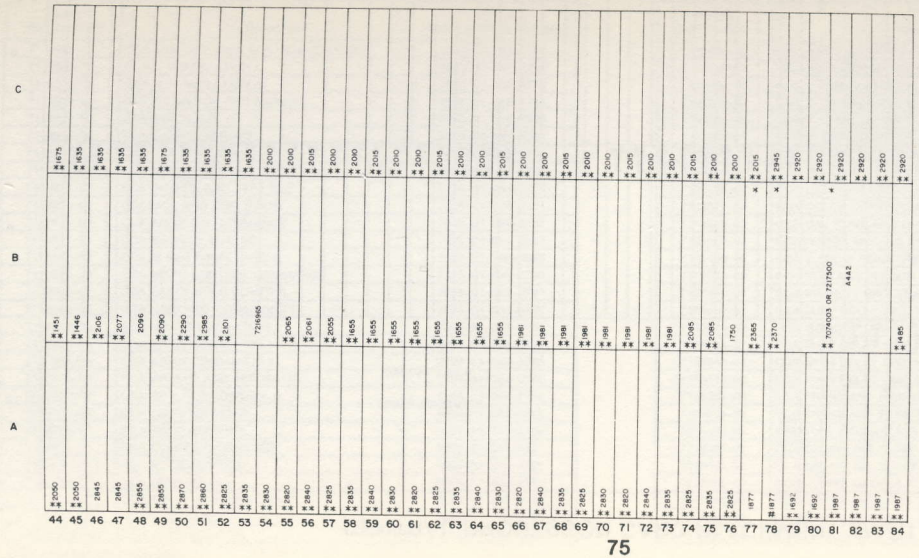
NOTE:

1. UNLESS OTHERWISE SPECIFIED PREFIX ALL CENTRAL PROCESSOR MODULE PART NUMBERS WITH 711___.
2. FOR PRINTED CIRCUIT INTERCHANGEABILITY DATA REFER TO DRAWING 7073474.

*3. PREFIX WITH 715___.

**4. ESD SENSITIVE, USE ESD PRECAUTIONARY PROCEDURES WHEN HANDLING.

CENTRAL PROCESSOR CARD PLACEMENT, PART 2



NOTE:

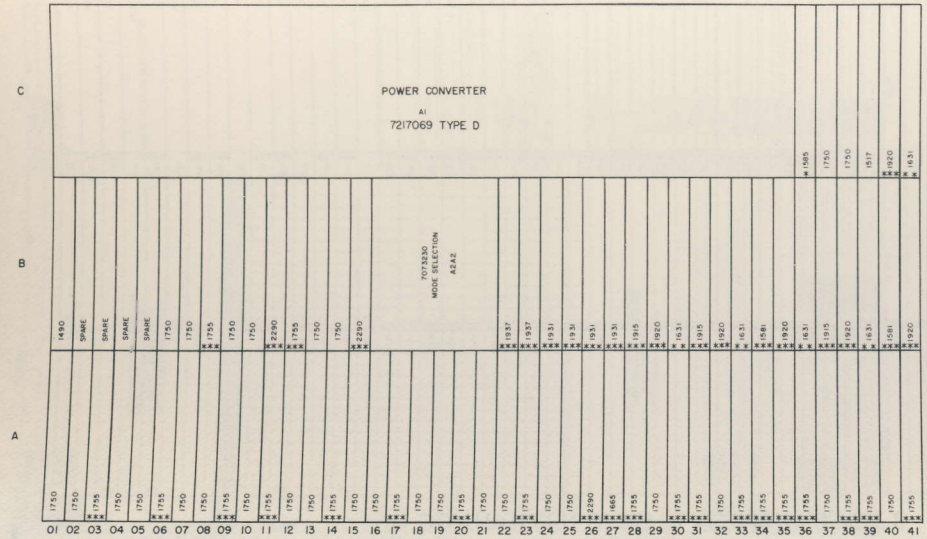
1. UNLESS OTHERWISE SPECIFIED PREFIX ALL CENTRAL PROCESSOR MODULE PART NUMBERS WITH 711___.
2. FOR PRINTED CIRCUIT INTERCHANGEABILITY REFER TO DRAWING 7073474.

*3. PRINTED CIRCUIT ASSEMBLIES IN LOCATIONS A4A77B AND A4A78B ARE NOT USED WITH NDRO 7217500.

**4. ESD SENSITIVE, USE ESD PRECAUTIONARY PROCEDURES WHEN HANDLING.

#5. A 7111818 CIRCUIT CARD ASSEMBLY WILL BE INSTALLED IN THIS CARD LOCATION IF FC9 CPU IS INCORPORATED.

I/O CONTROLLER CARD PLACEMENT, PART 1



NOTE:

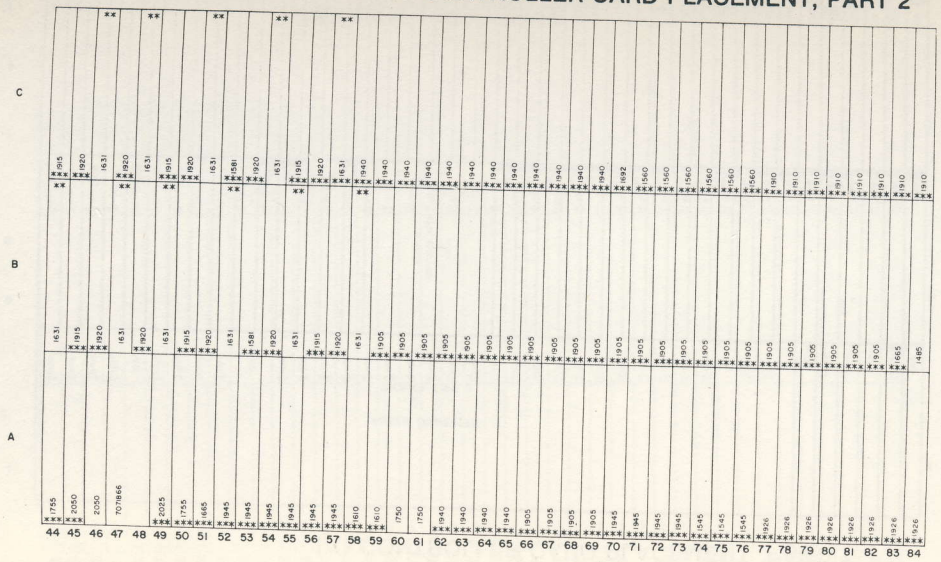
1. UNLESS OTHERWISE SPECIFIED PREFIX ALL I/O CONTROLLER MODULE PART NUMBERS WITH 711___.
2. FOR PRINTED CIRCUIT INTERCHANGEABILITY REFER TO DRAWING 7073474.

*3. PREFIX WITH 715___.

**4. MAY HAVE 7111005 CIRCUIT CARD ASSEMBLY IN THIS LOCATION IF FC-8 IS NOT INSTALLED.

***5. ESD SENSITIVE, USE PRECAUTIONARY PROCEDURES WHEN HANDLING.

I/O CONTROLLER CARD PLACEMENT, PART 2



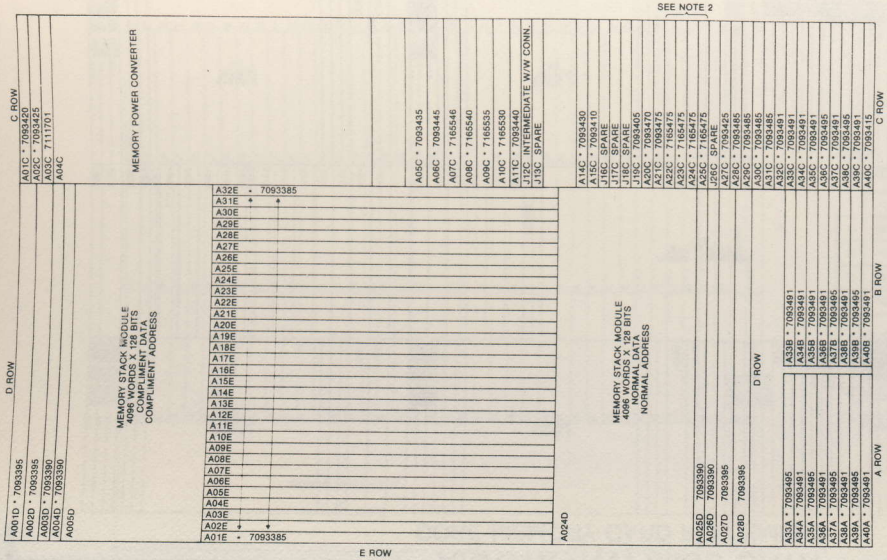
NOTE:

1. UNLESS OTHERWISE SPECIFIED PREFIX ALL I/O CONTROLLER MODULE PART NUMBERS WITH 711____.
2. FOR PRINTED CIRCUIT INTERCHANGEABILITY DATA REFER TO DRAWING 7073474.

**3. MAY HAVE 7111005 CIRCUIT CARD ASSEMBLY IN THIS LOCATION IF FC-8 IS NOT INSTALLED.

***4. ESD SENSITIVE, USE PRECAUTIONARY PROCEDURES WHEN HANDLING.

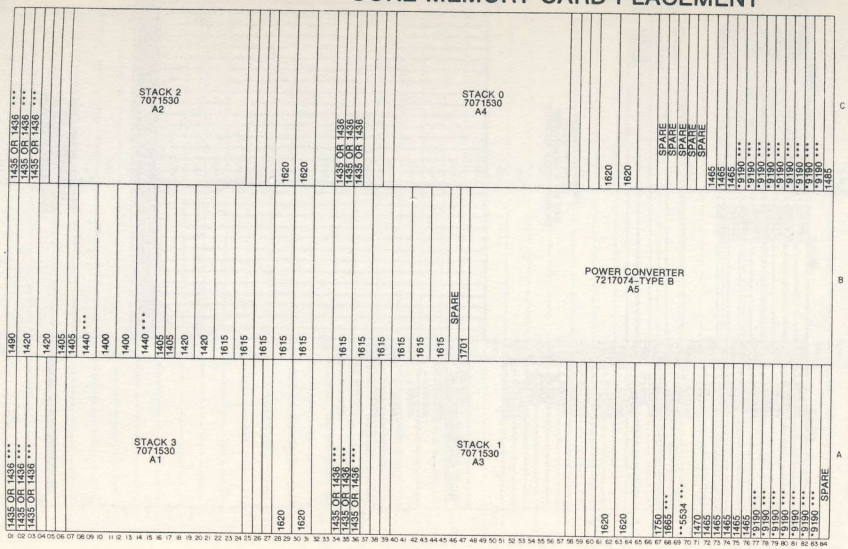
MATED FILM MEMORY CARD PLACEMENT



NOTE:

1. * ESD SENSITIVE, USE ESD PRECAUTIONARY PROCEDURES WHEN HANDLING.
2. CARD TYPE IS 7165476 IF FC9 DDM IS INCORPORATED.

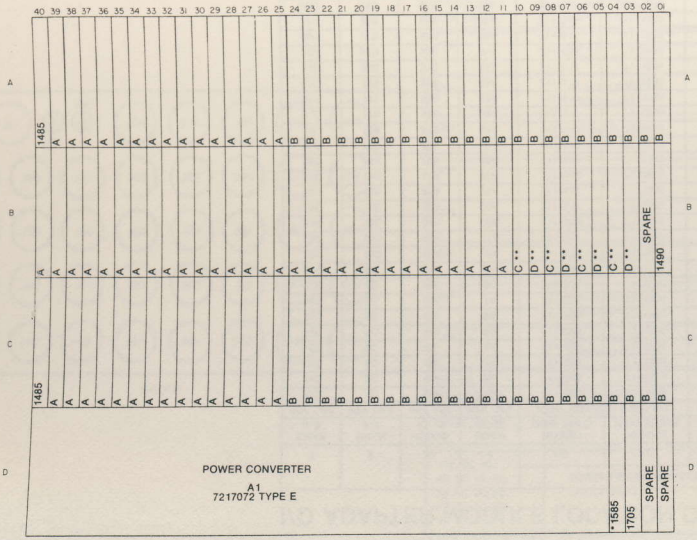
CORE MEMORY CARD PLACEMENT



NOTE:

1. UNLESS OTHERWISE SPECIFIED, PREFIX ALL MEMORY MODULE PART NUMBERS WITH 711_ _ _ _.
2. FOR PRINTED CIRCUIT INTERCHANGEABILITY DATA REFER TO DRAWING 7073474.
3. *PREFIX WITH 713_ _ _ _ _ _ _.
4. **PREFIX WITH 716_ _ _ _ _ _.
5. ***ESD SENSITIVE, USE ESD PRECAUTIONARY PROCEDURES WHEN HANDLING.

I/O ADAPTER CARD PLACEMENT



NOTES:

1. CARD TYPE (UNLESS OTHERWISE SPECIFIED)

	-3V	-15V	+3V
A	1517	1530	3336
B	1505	1520	3330
C	1511	1527	1511
D	1540	1535	1540

2. UNLESS OTHERWISE SPECIFIED PREFIX ALL I/O ADAPTER MODULE PART NUMBERS WITH 711_ _ _ _.
3. FOR PRINTED CIRCUIT INTERCHANGEABILITY DATA REFER TO DRAWING 7073474.

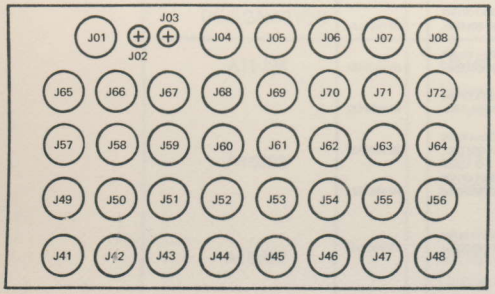
*4. PREFIX WITH 715_ _ _ _.

**5. ESD SENSITIVE, USE ESD PRECAUTIONARY PROCEDURES WHEN HANDLING.

I/O ADAPTER MODULE LOCATION CHART

1	2	3	4	CARD LIST PART NUMBERS		
				KIT	KIT	KIT
CHAN 0-3	CHAN 4-7	CHAN 10-13	CHAN 14-17	7073301 (NEG FAST)	7073302 (NEG SLOW)	7073303 (POS FAST)
REF DES	REF DES	REF DES	REF DES	PART NO.	PART NO.	PART NO.
13C	1C	13A	1A	7111505	7111520	7113330
14C	2C	14A	2A	7111505	7111520	7113330
15C	3C	15A	3A	7111505	7111520	7113330
16C	4C	16A	4A	7111505	7111520	7113330
17C	5C	17A	5A	7111505	7111520	7113330
18C	6C	18A	6A	7111505	7111520	7113330
19C	7C	19A	7A	7111505	7111520	7113330
20C	8C	20A	8A	7111505	7111520	7113330
21C	9C	21A	9A	7111505	7111520	7113330
22C	10C	22A	10A	7111505	7111520	7113330
23C	11C	23A	11A	7111505	7111520	7113330
24C	12C	24A	12A	7111505	7111520	7113330
25C	11B	26B	25A	7111517	7111530	7113336
26C	12B	27B	26A	7111517	7111530	7113336
27C	13B	28B	27A	7111517	7111530	7113336
28C	14B	29B	28A	7111517	7111530	7113336
29C	15B	30B	29A	7111517	7111530	7113336
30C	16B	31B	30A	7111517	7111530	7113336
31C	17B	32B	31A	7111517	7111530	7113336
32C	18B	33B	32A	7111517	7111530	7113336
33C	19B	34B	33A	7111517	7111530	7113336
34C	20B	35B	34A	7111517	7111530	7113336
35C	21B	36B	35A	7111517	7111530	7113336
36C	22B	37B	36A	7111517	7111530	7113336
37C	23B	38B	37A	7111517	7111530	7113336
38C	24B	39B	38A	7111517	7111530	7113336
39C	25B	40B	39A	7111517	7111530	7113336
9B	7B	5B	3B	7111540	7111535	7111540
10B	8B	6B	4B	7111511	7111527	7111511

AN/UYK-7(V) CABLE AND INTERFACE CONNECTIONS



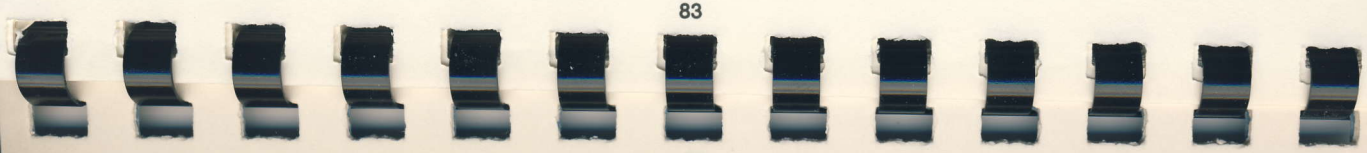
FRONT

CONNECTOR REF. DESIG.	CONNECTOR PART NUMBER	MATING CONNECTOR PART NUMBER	FUNCTION
J01	MS 3102R20-15P (905418-04)	MS 3106R20-15S (905411-04)	PRIMARY POWER
J05	M81511/01EF01S2 (7902701-01)	M81511/06EF01P2 (7902700-01)	CONTROL INDICATE SIGNAL MAINTENANCE CONSOLE UNIT
J06	M81511/01EF01S3 (7902701-02)	M81511/063F01P3 (7902700-02)	CONTROL INDICATE SIGNAL MAINTENANCE CONSOLE UNIT
J07	M81511/01EF01S4 (7902701-03)	M81511/06EF01P4 (7902700-03)	CONTROL INDICATE SIGNAL MAINTENANCE CONSOLE UNIT
J08	M81511/01EF01S5 (7902701-04)	M81511/06EF01P5 (7902700-04)	CONTROL INDICATE SIGNAL MAINTENANCE CONSOLE UNIT
J04	M81511/01EF01S6 (7902701-05)	M81511/06EF01P6 (7902700-05)	SYSTEM MONITOR PANEL OR REMOTE OPERATING UNIT
J02	MS 3112E8-4S (7900533-00)	MS 3116F8-4P (7901820-00)	EXTERNAL CLOCK (INPUT)
J03	MS 3112E8-4S (7900533-00)	MS 3116F8-4P (7901820-00)	EXTERNAL CLOCK (OUTPUT)
J41, 43, 45, 47, 49, 51, 53, 55, 57, 59, 61, 63, 65, 67, 69, 71	M81511/01EF01P1 (7902698-00)	M81511/06EF01S1 (7902699-00)	INPUT CHANNELS
J42, 44, 46, 48, 50, 52, 54, 56, 58, 60, 62, 64, 66, 68, 70, 72	M81511/01EF01P2 (7902698-01)	M8155/06EF01S2 (7902699-01)	OUTPUT CHANNELS

85-PIN CABLE END FABRICATION CONNECTOR KITS

SPERRY KIT P/N	CONNECTOR PLUG P/N	USED ON
7214384-00	7902699-00 M81511/06EF01S1	Computer input jacks A1J41: J43, J45, J47, J49, J51, J53, J55, J57, J59, J61, J63, J65, J67, J69, J71 Maintenance console jacks A19J03, A19J02, A19J01
7214384-01	7902699-01 **M81511/06EF01S2**	Computer output jacks A1J42: J44, J46, J48, J50, J52, J54, J56, J58, J60, J62, J64, J66, J68, J70, J72
7214384-04	7902699-03 M81511/06EF01S4	Maintenance console jack A19J04
7214384-05	7902700-01 M81511/06EF01P2	Cabinet jack A8J05 Maintenance console cable W4
7214384-06	7902700-02 M81511/06EF01P3	Cabinet jack A8J06 Maintenance console cable W3
7214384-07	7902700-03 M81511/06EF01P4	Cabinet jack A8J07 Maintenance console cable W2
7214384-08	7902700-04 M81511/06EF01P5	Cabinet jack A8J08 Maintenance console cable W1
7214384-09	7902700-05 M81511/06EF01P6	Cabinet jack A8J04 for ROCU cable
7214384-11	7902699-03 M81511/06EF01S4	ROCU jack J01

NOTES:
1. Connector plug 7902700-XX uses male pins and connector plug 7902699-XX uses female pins.
2. Connector kit 7214384-11 only includes 26 ea. sealing plugs 7902852-00 for environmentally sealing unwired pins in plug. For other kits, they must be ordered separately.



MAINTENANCE CONSOLE/TEST SET CONNECTORS

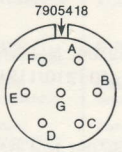
MAINTENANCE CONSOLE CONNECTOR REFERENCE DESIGNATION	MAINTENANCE CONSOLE CONNECTOR PART NUMBER	MATING CABLE CONNECTOR PART NUMBER	CABLE CONNECTOR REFERENCE DESIGNATION
A19J04	M81511/01EF01P4 Univac P/N 7902698-03	M81511/06EF01S4 Univac P/N 7902699-03	W1P2
A19J03	M81511/01EF01P1 Univac P/N 7902698-00	M81511/06EF01S1 Univac P/N 7902699-00	W2P2
A19J02	M81511/01EF01P1 Univac P/N 7902698-00	M81511/06EF01S1 Univac P/N 7902699-00	W3P2
A19J01	M81511/01EF01P1 Univac P/N 7902698-00	M81511/06EF01S1 Univac P/N 7902699-00	W4P2

NOTE: Maintenance Console/Test Set cables are supplied with each computer set.

PRIMARY POWER CONNECTOR

Pin assignments for primary input power connector J1 (115V and 208V)

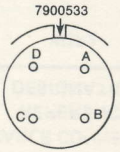
UYK-7(V) Jack and Pin	115-Volt Primary Power Function
J01-A	Phase A
J01-B	Unused
J01-C	Phase B
J01-D	Unused
J01-E	Phase C
J01-F	Unused
J01-G	Neutral
UYK-7(V) Jack and Pin	**208-Volt Primary Power Function**
J01-A	Phase A
J01-B	Unused
J01-C	Phase B
J01-D	Unused
J01-E	Phase C
J01-F	Unused
J01-G	Neutral



EXTERNAL CLOCK CONNECTORS (CABINET) INPUT/OUTPUT

The pin assignments for jack A8J02 and A8J03 are as follows:

A8J02 PIN	FUNCTION
A	External RTC
B	External RTC Return
C	Shield Ground
D	Unused



INPUT/OUTPUT CONNECTOR PIN/SIGNAL ASSIGNMENTS

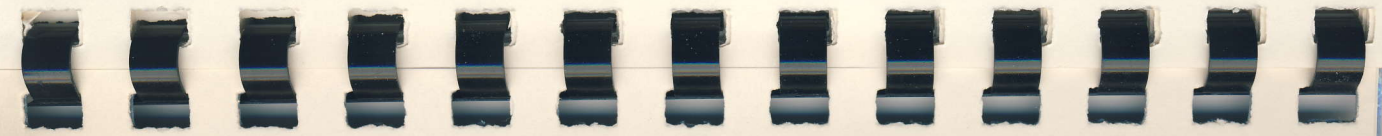
INPUT	
JACK AND PIN	FUNCTIONS
–	PARALLEL DATA INPUT
JXX-01 JXX-06	INPUT DATA REQ. RETURN
JXX-02 JXX-07	INPUT ACK. RETURN
JXX-03 JXX-08	EXT. INTRPT. REQ. RETURN
JXX-04 JXX-09	EXT. INTRPT. ENABLE RETURN
JXX-05 JXX-12	DATA BIT 31 RETURN
JXX-10 JXX-11	DATA BIT 32 (UNUSED) RETURN (UNUSED)
JXX-19 JXX-27	DATA BIT 34 (UNUSED) RETURN (UNUSED)
JXX-20 JXX-28	SPARE SPARE
JXX-13 JXX-21	DATA BIT 00 RETURN
JXX-14 JXX-22	DATA BIT 01 RETURN

OUTPUT	
JACK AND PIN	FUNCTIONS
–	PARALLEL DATA OUTPUT
JXX-01 JXX-06	OUTPUT ACKNOWLEDGE RETURN
JXX-02 JXX-07	OUTPUT DATA REQUEST RETURN
JXX-03 JXX-08	EXT. FUNCT ACK RETURN
JXX-04 JXX-09	EXT. FUNCT REQ RETURN
JXX-05 JXX-12	DATA BIT 31 RETURN
JXX-10 JXX-11	DATA BIT 32 (UNUSED) RETURN (UNUSED)
JXX-19 JXX-27	DATA BIT 34 (UNUSED) RETURN (UNUSED)
JXX-20 JXX-28	SPARE SPARE
JXX-13 JXX-21	DATA BIT 00 RETURN
JXX-14 JXX-22	DATA BIT 01 RETURN

INPUT/OUTPUT CONNECTOR PIN/SIGNAL ASSIGNMENTS (continued)

INPUT	
JACK AND PIN	FUNCTIONS
JXX-15 JXX-23	DATA BIT 02 RETURN
JXX-16 JXX-24	DATA BIT 03 RETURN
JXX-17 JXX-25	DATA BIT 04 RETURN
JXX-18 JXX-26	DATA BIT 05 RETURN
JXX-29 JXX-39	DATA BIT 06 RETURN
JXX-30 JXX-40	DATA BIT 07 RETURN
JXX-31 JXX-41	DATA BIT 08 RETURN
JXX-32 JXX-42	DATA BIT 09 RETURN
JXX-33 JXX-43	DATA BIT 10 RETURN
JXX-34 JXX-44	DATA BIT 11 RETURN
JXX-35 JXX-45	DATA BIT 12 RETURN

OUTPUT	
JACK AND PIN	FUNCTIONS
JXX-15 JXX-23	DATA BIT 02 RETURN
JXX-16 JXX-24	DATA BIT 03 RETURN
JXX-17 JXX-25	DATA BIT 04 RETURN
JXX-18 JXX-26	DATA BIT 05 RETURN
JXX-29 JXX-39	DATA BIT 06 RETURN
JXX-30 JXX-40	DATA BIT 07 RETURN
JXX-31 JXX-41	DATA BIT 08 RETURN
JXX-32 JXX-42	DATA BIT 09 RETURN
JXX-33 JXX-43	DATA BIT 10 RETURN
JXX-34 JXX-44	DATA BIT 11 RETURN
JXX-35 JXX-45	DATA BIT 12 RETURN



JXX-36 JXX-46	DATA BIT 13 RETURN
JXX-37 JXX-47	DATA BIT 14 RETURN
JXX-49 JXX-58	DATA BIT 15 RETURN
JXX-50 JXX-59	DATA BIT 16 RETURN
JXX-51 JXX-60	DATA BIT 17 RETURN
JXX-52 JXX-61	DATA BIT 18 RETURN
JXX-53 JXX-62	DATA BIT 19 RETURN
JXX-54 JXX-63	DATA BIT 20 RETURN
JXX-55 JXX-64	DATA BIT 21 RETURN
JXX-56 JXX-65	DATA BIT 22 RETURN
JXX-57 JXX-66	DATA BIT 23 RETURN
JXX-67 JXX-75	DATA BIT 24 RETURN
JXX-68 JXX-76	DATA BIT 25 RETURN
JXX-69 JXX-77	DATA BIT 26 RETURN

JXX-36 JXX-46	DATA BIT 13 RETURN
JXX-37 JXX-47	DATA BIT 14 RETURN
JXX-49 JXX-58	DATA BIT 15 RETURN
JXX-50 JXX-59	DATA BIT 16 RETURN
JXX-51 JXX-60	DATA BIT 17 RETURN
JXX-52 JXX-61	DATA BIT 18 RETURN
JXX-53 JXX-62	DATA BIT 19 RETURN
JXX-54 JXX-63	DATA BIT 20 RETURN
JXX-55 JXX-64	DATA BIT 21 RETURN
JXX-56 JXX-65	DATA BIT 22 RETURN
JXX-57 JXX-66	DATA BIT 23 RETURN
JXX-67 JXX-75	DATA BIT 24 RETURN
JXX-68 JXX-76	DATA BIT 25 RETURN
JXX-69 JXX-77	DATA BIT 26 RETURN

INPUT/OUTPUT CONNECTOR PIN/SIGNAL ASSIGNMENTS (continued)

INPUT	
JACK AND PIN	FUNCTIONS
JXX-70 JXX-78	DATA BIT 27 RETURN
JXX-71 JXX-79	DATA BIT 28 RETURN
JXX-72 JXX-80	DATA BIT 29 RETURN
JXX-73 JXX-81	DATA BIT 30 RETURN
JXX-38 JXX-48	SPARE SPARE
JXX-82 JXX-83	DATA BIT 33 (UNUSED) RETURN (UNUSED)
JXX-84 JXX-85	DATA BIT 35 (UNUSED) RETURN (UNUSED)
NONE NONE	NONE NONE
NONE NONE	NONE NONE
NONE NONE	NONE NONE
JXX-74	SHIELD

OUTPUT	
JACK AND PIN	FUNCTIONS
JXX-70 JXX-78	DATA BIT 27 RETURN
JXX-71 JXX-79	DATA BIT 28 RETURN
JXX-72 JXX-80	DATA BIT 29 RETURN
JXX-73 JXX-81	DATA BIT 30 RETURN
JXX-38 JXX-48	SPARE SPARE
JXX-82 JXX-83	DATA BIT 33 (UNUSED) RETURN (UNUSED)
JXX-84 JXX-85	DATA BIT 35 (UNUSED) RETURN (UNUSED)
NONE NONE	NONE NONE
NONE NONE	NONE NONE
NONE NONE	NONE NONE
JXX-74	SHIELD

REMOTE OPERATOR'S CONTROL UNIT (ROCU) CONNECTORS

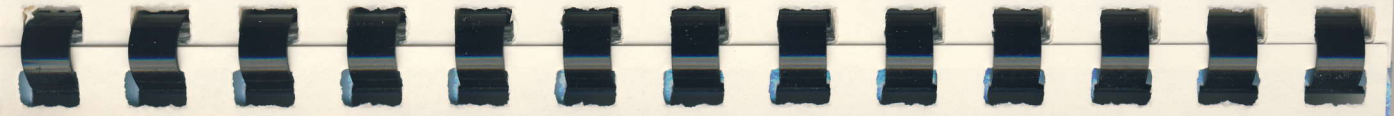
ROCU CONNECTORS REFERENCE DESIGNATION	ROCU CONNECTOR PART NUMBER	MATING CABLE CONNECTOR PART NUMBER	FUNCTION
J01	M81511/01EF01P4 (7902698-03)	M81511/01EF01S4 (7902699-03)	Control Signals and power
J02	MS3102E-16S-8P (7905438-00)	MS3106F-16S-8S (7905467-00)	External overtemp horn

P/N 7071687-00 Remote Operator's Control Unit
P/N 7071687-02 Remote Operator's Control Unit with external overtemp horn

PIN ASSIGNMENTS FOR SIGNALS IN ROCU TO REMOTE OVERTEMP HORN

ROCU CONNECTOR J2	FUNCTION	PIN ASSIGNMENTS J07 (7905438)
J2-A	Overtemp Remote	
J2-B	Overtemp Remote	
J2-C	Ground	

NOTE: An Overtemp condition closes relay contacts in the ROCU, thereby shorting pins A and B together.



PIN ASSIGNMENTS FOR SIGNALS IN ROCU TO UYK–7(V) CABLE

UYK-7(V) JACK AND PIN	2U-45 CABLE RECOMMENDED TWISTED PAIR	ROCU JACK AND PIN	FUNCTION	
–	–	–	RMTE CMPTR CTL	1
J04-02	PAIR 01	J01-02	SIGNAL GND	2
J04-01		J01-01	+90 VDC POWER	3
J04-04	PAIR 02	J01-04	SIGNAL GND	4
J04-03		J01-03	+5VDC POWER	5
J04-06	PAIR 03	J01-06	SIGNAL GND	6
J04-05		J01-05	+28VDC POWER	7
J04-08	PAIR 04	J01-08	SIGNAL GND	8
J04-07		J01-07	-5VDC POWER	9
J04-10	PAIR 05	J01-10	SPARE	10
J04-09		J01-09	SPARE	11
NONE	PAIR 06	NONE	NOT TERMINATED	12
NONE		NONE	NOT TERMINATED	13
J04-13	PAIR 07	J01-13	RUN IND RTN	14
J04-12		J01-12	RUN IND	15
J04-15	PAIR 08	J01-15	SIGNAL GND	16
J04-14		J01-14	LOW OVERTEMP BUS	17
J04-17	PAIR 09	J01-17	SIGNAL GND	18
J04-16		J01-16	POWER FAULT IND	19
J04-19	PAIR 10	J01-19	SIGNAL GND	20
J04-18		J01-18	PROGRAM FAULT IND	21
NONE	PAIR 11	NONE	NOT TERMINATED	22
J04-20		J01-20	SPARE	23
J04-22	PAIR 12	J01-22	SIGNAL GND	24
J04-21		J01-21	HARDWARE FAULT IND	25
J04-24	PAIR 13	J01-24	SIGNAL GND	26
J04-23		J01-23	STOP 5 IND	27
J04-26	PAIR 14	J01-26	SIGNAL GND	28
J04-25		J01-25	STOP 6 IND	29
J04-28	PAIR 15	J01-28	SPARE	30
J04-27		J01-27	SPARE	31
J04-30	PAIR 16	J01-30	SPARE	32
J04-29		J01-29	SPARE	33
J04-32	PAIR 17	J01-32	STOP 7 IND	34
J04-31		J01-31	SIGNAL GND	35
J04-34	PAIR 18	J01-34	STOP 4 IND	36
J04-33		J01-33	SIGNAL GND	37
J04-36	PAIR 19	J01-36	SPARE	38
J04-35		J01-35	SIGNAL GND	39
J04-38	PAIR 20	J01-38	SPARE	40
J04-37		J01-37	SPARE	41
J04-40	PAIR 21	J01-40	SPARE	42
J04-39		J01-39	SPARE	43
J04-42	PAIR 22	J01-42	SPARE	44
J04-41		J01-41	SIGNAL GND	45
J04-44	PAIR 23	J01-44	SPARE	46
J04-43		J01-43	SIGNAL GND	47

UYK-7(V) JACK AND PIN	2U-45 CABLE RECOMMENDED TWISTED PAIR	ROCU JACK AND PIN	FUNCTION	
J04-46	PAIR 24	J01-46	SPARE	48
J04-45		J01-45	SIGNAL GND	49
J04-48	PAIR 25	J01-48	SPARE	50
J04-47		J01-47	SPARE	51
J04-50	PAIR 26	J01-50	ON LINE RTN	52
J04-49		J01-49	ON LINE SEL	53
J04-52	PAIR 27	J01-52	RUN RTN	54
J04-51		J01-51	RUN SELECT	55
J04-54	PAIR 28	J01-54	REMOTE RTN 1	56
J04-53		J01-53	AUTO RECVY SEL	57
J04-56	PAIR 29	J01-56	MANUAL RTN	58
J04-55		J01-55	MANUAL SEL	59
J04-58	PAIR 30	J01-58	SPARE	60
J04-57		J01-57	SPARE	61
–	–			62
J04-60	PAIR 31	J01-60	BOOTSTRAP 1 RTN	63
J04-59		J01-59	BOOTSTRAP 1 SEL	64
J04-62	PAIR 32	J01-62	BOOTSTRAP 2 RTN	65
J04-61		J01-61	BOOTSTRAP 2 SEL	66
J04-64	PAIR 33	J01-64	RMTE MSTR CLEAR RTN	67
J04-63		J01-63	RMTE MSTR CLEAR SEL	68
J04-66	PAIR 34	J01-66	RMTE RTN 1	69
J04-65		J01-65	STOP 5 SEL	70
NONE	PAIR 35	NONE	NOT TERMINATED	71
J04-67		J01-67	SPARE	72
J04-69	PAIR 36	J01-69	STOP 6 SEL	73
J04-68		J01-68	STOP 6 RTN	74
J04-71	PAIR 37	J01-71	STOP 7 SEL	75
J04-70		J01-70	STOP 7 RTN	76
J04-73	PAIR 38	J01-73	JUMP 1 SEL	77
J04-72		J01-72	JUMP 1 RTN	78
J04-75	PAIR 39	J01-75	SPARE	79
J04-74		J01-74	SPARE	80
J04-77	PAIR 40	J01-77	JUMP 2 SEL	81
J04-76		J01-76	JUMP 2 RTN	82
J04-79	PAIR 41	J01-79	JUMP 3 SEL	83
J04-78		J01-78	JUMP 3 RTN	84
J04-81	PAIR 42	J01-81	STOP SEL	85
J04-80		J01-80	STOP RTN	86
J04-83	PAIR 43	J01-83	RUN NEUTRAL RTN	87
J04-82		J01-82	RUN NEUTRAL SEL	88
J04-85	PAIR 44	J01-85	SPARE	89
J04-84		J01-84	SPARE	90
NONE	PAIR 45	NONE	NOT TERMINATED	91
NONE		NONE	NOT TERMINATED	92
J04-11	SHIELD	J01-11	CHASSIS GROUND	93