HIGH-SPEED SERIAL I/O INTERCONNECT SYSTEM

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1. INTRODUCTION

Currently, most computer input/output communication at distances up to 500 feet is achieved using parallel data transfer over multiwire twisted pair cable. This type of interconnect system is limited in data rate, interface distance, and requires large multipin connectors and bulky cable. These problems have been minimized in a high-speed serial I/O system using RF/optical serial transmission over coaxial or fiber optic cable. The new system provides a large length interface distance, simplifies channel switching, and is adaptible to Time Division Multiplex (TDM) communication links and data buses.

This paper describes a high-speed retrofit serial I/O interconnect system. The system is backwards compatible with current parallel interfaces and is being implemented as part of a Centrally Controlled Interconnection System (CCIS) for automatic reconfiguration of computer/peripheral complexes. CCIS consists of a duplex 320 and 320 I/O switch matrix and is described in a complementary paper entitled "So Your Computer Center Has a Switching Problem" by J. L. Fritz.

2. BACKGROUND

There have been three generations of Sperry Univac military computers developed with little enhancement in I/O communication other than a nominal reduction in size through the use of smaller connectors and hybrid line driver/receiver circuitry. Use of higher-speed (fast interface) line driver/receiver circuits has been implemented but with a corresponding reduction in interconnect distance (300 feet maximum). Each succeeding generation has resulted in a substantial reduction in processor size, but now further size reduction is being limited by the space required for I/O connectors and cable. Some special purpose serial I/O systems have been developed, but they have not had general application because of the lack of compatibility with peripheral equipment designed for a parallel interface.

Today's increasing requirements call for longer interface distances (up to 1000 feet), I/O channel switching, and interconnect bus structures accommodating several subscribers. These factors and others have prompted the development of a retrofit serial I/O interconnect system. The system must be applicable to existing systems and can be implemented in new systems and still retain compatibility with current parallel interface equipment.

3. SERIAL I/O EVOLUTION

Successful implementation of serial I/O interconnect systems, on a wide-spread basis, will require both backward and forward compatibility of mixed systems. That is, both old and new computer and peripheral equipment will require use of external adapters for converting parallel interfaces to serial interfaces and vice-versa. This allows the customer the option of using his old equipment with the new until such time as he elects to replace the old equipment.

Maximum performance and economy are obtained when serial I/O is integral with the computer and peripheral equipment, but the first step is the development of an acceptable external converter for mixed system applications. This is the current phase of our development program in which external converters are used to convert both parallel interface computer and perhipheral equipment to a serial interconnect system.

4. RETROFIT CONVERTER DESIGN

Retrofit serial I/O, by definition, is the replacement of existing parallel I/O cables (two per channel) with a serial interface. (Figure 1). The parallel data is converted to a serial data stream for transmission over a single cable and reassembled in parallel format at the receiver. It is a retrofit interconnect system, in the sense that it is self-contained and no modifications to the processor and peripheral equipment are required.

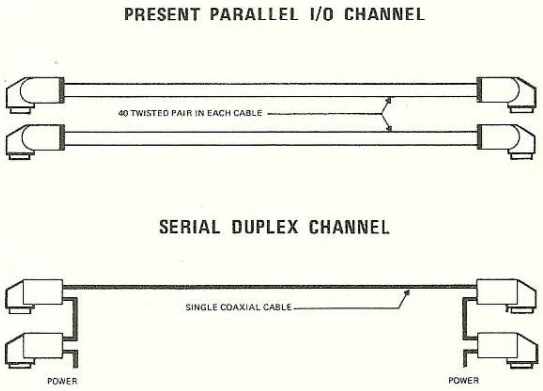


Figure 1. Retrofit Serial I/O

The unique features of the converter design are its packaging and transmission system which enables bidirectional communication over a single coaxial cable. Through the use of hybrid circuitry, the electronics have been packaged in a unit which can be plugged into existing parallel interface converter receptacles. A comparison of an 85 pin connector and twisted pair cable with the converter package and coaxial cable is shown in Figure 2. Moreover, the internal electronics module (Figure 3) is designed so that it can be mounted within the shell dimensions of other connector types. Converter units to fit three types of connector receptacles have been designed.

4.1. PARALLEL INTERFACE FORMAT

Sperry Univac Defense System Computer interfaces have been standardized and consist of up to 36 lines for data and four lines for control information for each direction of transmission. Two multiwire twisted pair cables and associated connectors are used for the interconnect system. Slow or fast line driver/receivers may be used to provide maximum word transfer rates of 40 and 167K words per second, respectively. However, in practice, maximum data rates are achieved only in block transfers without acknowledgement between words. Typical maximum request/acknowledge transfer rates are approximately half that of block transfers.

4.2. SERIAL I/O BLOCK DIAGRAM

The primary functions of the system are shown in Figure 4 and consist of the interface adapter, converter and control logic, and the transceiver.

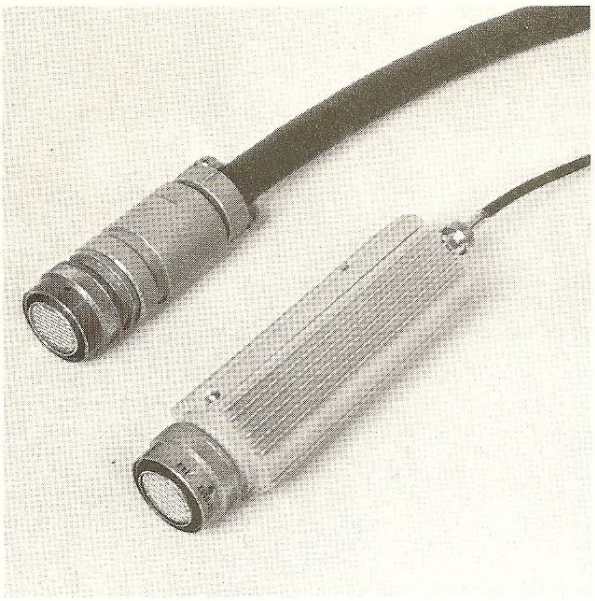


Figure 2. Cable Connector and Serial Converter Module

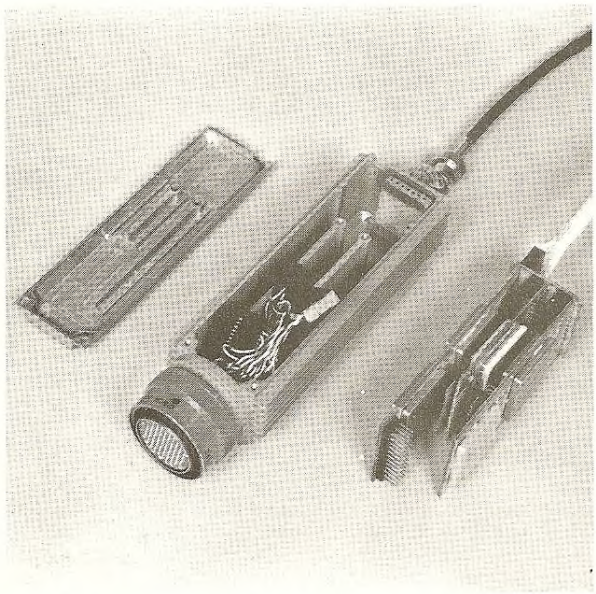


Figure 3. Retrofit Serial Converter Module Assembly

4.2.1. INTERFACE ADAPTER. The interface adapter contains conventional line/driver receiver circuitry compatible with the I/O characteristics of the computer/peripheral equipment. This function requires the most circuitry (11 hybrids) since 80 lines are either driven or terminated and occupies over half the package space. The adapter is eliminated in an integral serial I/O system because the converter interfaces directly at the logic level of the I/O section and line drivers/receivers are not required. Besides reduction in circuitry, integral serial I/O has higher word transfer rates since delays through the line driver/receiver circuits are eliminated.

4.2.2 CONVERTER. The converter provides the serialization and parallel assembly process including the interleaving of control information within the serial data stream. The converter operates at a 25 Mbaud rate and has two inputs and outputs. It accepts 40 parallel inputs from the interface adapter and converts them to a non-return to zero (NRZ) data stream which drives the transceiver. It accepts an NRZ code from the transceiver and converts it to a 40 line parallel output. The circuitry is contained within eight 1" X 1" hybrid packages.

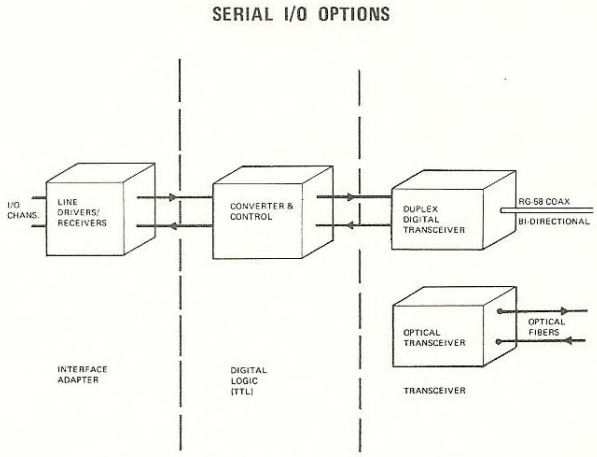


Figure 4. Serial I/O Block Diagram

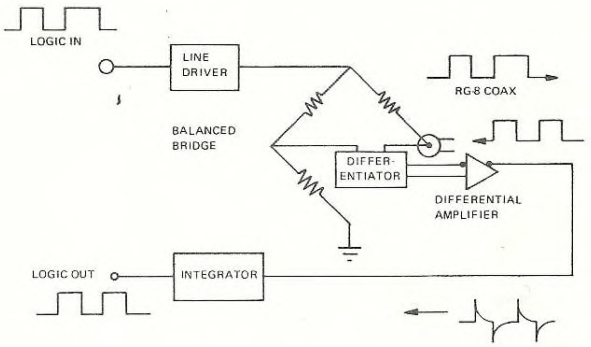


Figure 5. Transceiver Schematic

4.2.3 TRANSCEIVER. Two types of transceiver developments have been pursued of which the duplex digital transceiver is used in production systems. It provides simultaneous bidirectional communication over a single coaxial cable.

Development of an optical transceiver for use with fiber bundle cable is also in process as an option to the coaxial cable system. Fiber optic systems are of extreme interest in military applications where secure communications and immunity to high levels of interference are required. Both types of transceivers and their media are discussed in detail in the following section.

5. I/O TRANSMISSION SYSTEMS

This section provides design detail of the duplex digital transceiver, digital transmission format, and development work on optical transceivers and fiber optic cable.

5.1 DUPLEX DIGITAL TRANSCEIVER

The duplex digital transceiver is a baseband transmission system in which bidirectional communication is achieved through the use of a balanced bridge (Figure 5). One of the legs of the bridge is the 50 ohm transmission cable. Isolation of the transmit/receive signals is obtained by picking off the receive signal from the balance

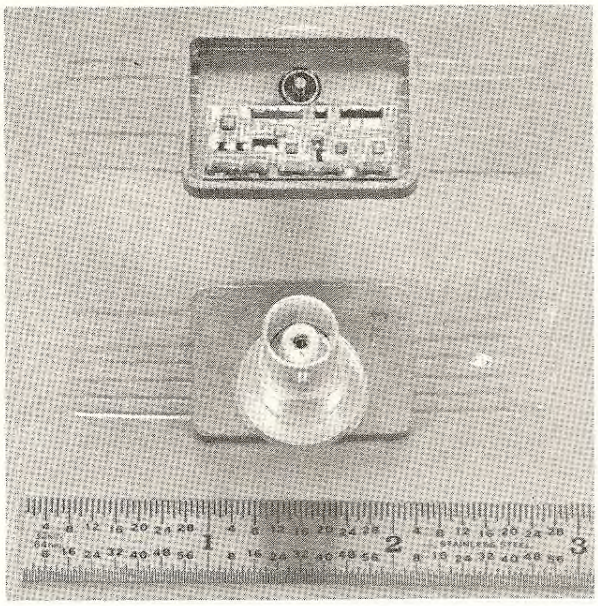


Figure 6. Hybrid Transceiver Module

balanced arms of the bridge. The circuit has been packaged in hybrid form (Figure 6) which has enabled precise balancing of the bridge and an isolation of transmit/receive signals of 35 db. The circuit contains three active components consisting of Emitter Coupler Logic (ECL) driver (MC 1011), differential amplifier (n A733), and ECL Schmitt Trigger (MC 10116). The coaxial connector is mounted directly on the package resulting in a Voltage Standing Wave Ratio (VSWR) of less than 1.1:1 up to 100 MHz.

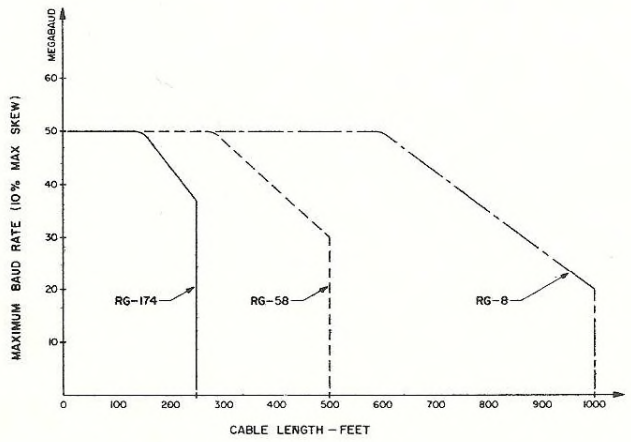


Figure 7. Interconnect System Performance

The transceiver accepts an NRZ input and reproduces it at the receive terminal. The NRZ signal is applied directly across the bridge through the ECL driver. The signal is differentiated at the input to the receiver so that the edges of the pulse waveform, only, are amplified and then fed to the Schmitt trigger for regeneration of the NRZ waveform.

Current production designs are operated at a 25 Mbaud rate over RG-58 triaxial cable at distances up to 500 feet. Longer interface distances and higher data rates up to 50 Mbaud can be accommodated by using larger cable. Data rate as a function of interface distance for three types of coaxial cable are shown in Figure 7. Maximum data rate is a function of the pulse skew of the transceiver and cable. Pulse skew has been minimized in the transceiver by the following design techniques:

1. ECL circuitry.
2. Differentiation receive network.
3. Matched line terminations.
4. Wide bandwidth amplifier.
5. Double inversion logic gates.
6. Precision Schmitt Trigger.

These techniques have resulted in a maximum transceiver skew per transceiver pair of less than $\pm$ 1 ns with the major skew due to the transmission cable itself.

A key attribute of this transmission system, essential to its application in a military environment, is its immunity to radiated and ground noise interference. The receiver input high-pass differentiating network effectively attenuates low frequency noise interference to the extent that the system can tolerate ground potential differences in excess of 15 volts peak up to 1 MHz. Moreover, its susceptibility to power line frequencies and low order harmonics exceeds 30 volts peak. (Figure 8). Similarly, its radiated susceptibility level using double shielded (TRIAX) cable exceeds 10 volt/meter which is 10 times the MIL-STD-461A requirement. In general, the system is susceptible to signals only within the passband of the differential amplifier (10-70 MHz) and double shielded cable provides sufficient isolation at these frequencies. The use of double shielded cable along with low transmission power levels also limits the radiated EMI to within MIL-STD-461A requirements.

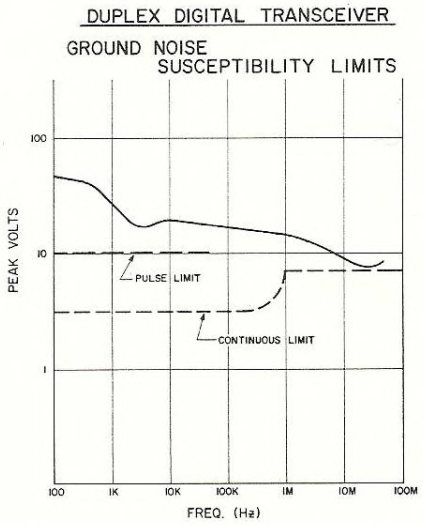


Figure 8. Transceiver Ground Noise Susceptibility

5.2. TRANSMISSION FORMAT

A byte transmission system based on a 25 Mbaud transmission rate is used with the following parameters and frame format of Figure 9.

40 ns Bit Interval

10 Bits/Byte

8 Bytes/Frame

400 ns Byte Interval

1 Sync Byte

7 Data Bytes

Start/Stop Sync Bits For Each Data Byte

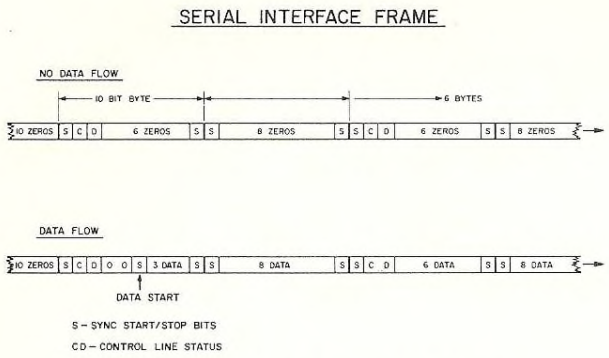


Figure 9. Serial Interface Frame

Essentially, the receiver recognizes the beginning of a frame by distinguishing a sync byte consisting of ten consecutive zeros. The beginning of each ten bit data byte consists of a start bit, which is a one, followed by eight data slots and a stop bit (0), which occupies the 10th slot. Control line sampling is interleaved in the data stream and is allocated to the 2nd and 3rd time slot of every other data byte. The word request control lines (CD) are sampled at 800 ns intervals or at a rate approximately three times that of the data lines. Transmission of control line status is continuous whether or not data is being transmitted. Data transmission commences immediately following a status change on the word initiation control lines which are monitored continuously. A data word can start within any data byte and continue until up to 36 data slots have been filled. Total word length (data, control, and synchronization bits) varies from 62 to 77 bits depending upon the point at which the word starts within the frame. This corresponds to a maximum serialization time of 3.08 μs. Other delays of the retrofit serial I/O system include 0.8 μs for fast interface line driver circuitry and an asynchronization delay of up to 0.8 μs for control line sampling.

5.3. FIBER OPTIC INTERCONNECT SYSTEMS

Fiber optic communication is a relatively new, rapidly evolving area of data transfer. Its advantages over a coaxial system include:

- Security (non-radiating)
- EMI immunity
- Electric isolation (non-conductor)
- Lightweight
- Low transmission loss
- Large bandwidth

Current limitations in application are cost, fiber length, bundle ruggedization, and lack of connector hardware. Progress is being made in all of these areas and in the development of the associated optical components for the transceivers.

Optic waveguides are constructed using a cylindrical core of a high-index of refraction glass surrounded by a cladding of a lower index of refraction. The light beam is confined to the waveguide by total internal reflection at the interface between the core and cladding, provided the launch angle is within the aperture of the guide. Pulse broadening or skew is caused by differences in launch angle and propagation time of rays within the beam. A ray with a low launch angle propagates along the axis of the cylinder and reaches the receiver sooner than one with a high launch angle which is reflected from the cylinder walls as it propagates down the guide. For multimode transmission, this factor limits maximum bandwidth to about 10^8 bits per second per kilometer. This limit is now being exceeded by waveguides in which the core has a graded index of refraction (index varies as a function of the distance from the axis) which equalizes path length and propagation time for all launch angles.

Our interest is primarily in multimode propagation using a high-performance light emitting diode (non-coherent emission) in the transmitter and a PIN diode as the detector. Higher bandwidths and data rates (10^{11} bits per second per kilometer) can be obtained using single mode fiber and laser (coherent) sources. Much development work is required in this area before application to interconnect systems.

Two types of fiber optic cable have been evaluated for the serial I/O interconnect system.

1. High loss fiber (Figure 10a) Galileo Electro-Optics Corp.- This cable contains 280 fibers, has a nominal attenuation of 350 db/km and an acceptance angle of 40 degrees. It is relatively low in cost ($0.50 per foot range with commercial grade cable sheath) and is suitable for short distance interconnects up to 200 feet. The bundle diameter is 45 mills with individual fiber diameters between two and three mills. As shown in Figure 10a, it is typical for many (up to 50%) of the fibers to be broken during fabrication and for individual fibers, to vary in degree of transmissability.

2. Low loss fiber (Figure 10b) Corning Glass Works - This bundle contains 22 fibers with a nominal attenuation of 20 db/km and is suitable for interconnect distances of 1000 feet. Its aperture angle is 8.5 degrees which requires precision in coupling the fiber to the LED source. Because of its high cost, the trend in cable development is to reduce the number of fibers (six or less) and combine these with a steel or plastic core for strength. This bundle would be encased in a protective epoxy with an outer shield. Ultimately, the goal of fiber bundle manufacturers is a cable comparable in size, strength, and cost to miniature coax (RG-174).

A typical optical interconnect system suitable for the 25 Mbaud rate of retrofit serial I/O is shown in Figure 11. It uses a GaAs LED as the emitter, a PIN photo diode detector followed by an amplifier and Schmitt trigger for conversion to a logic level output signal. The LED is driven by a driver circuit whose input is the serial data stream.

The GaAs LED source is compatible with the data rate and fiber optic cable characteristics. Its emission is near 900 nmeters and covers a 40 nmeter band. It has a cut-off frequency near 50 MHz.

External power conversion efficiencies are typically only 1% for these devices. An improvement in both bandwidth and conversion efficiency is expected in the near future so that higher data rates will be possible.

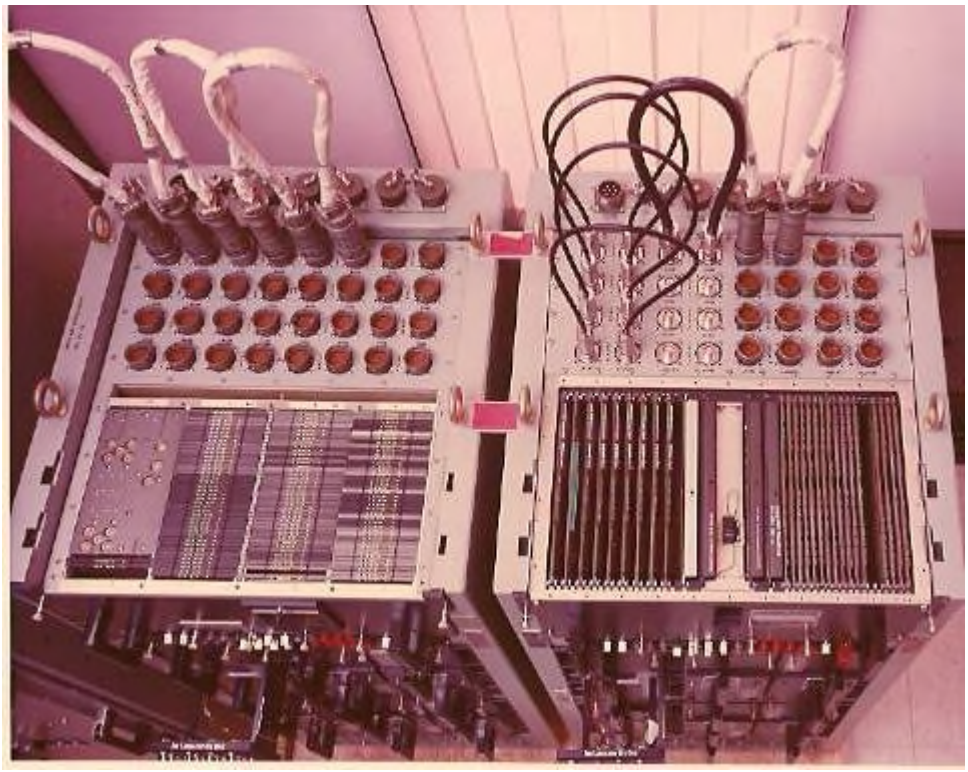
The choice of the light detector is dependent upon the source characteristics. Both PIN photodiodes and avalanche photodiodes have peak spectral responses near the 900 nmeter emission of a GaAs LED. When a

buses has emphasized the regenerative type system in which the data is regenerated at each station. The system then consists of a series of A-B links and is easily expandable or modified. High-speed transmission rates (20 Mbaud or higher) are favored in order that a burst mode or packet transmission technique can be employed. This simplifies the control of messages and reduces hardware costs. Regenerative type digital transmission systems are consistent with current trends in the communications industry for integration of both voice and data using a common Time Division Multiplex (TDM) serial channel.

7. SUMMARY

Current computer and peripheral equipment with a parallel I/O interface can be retrofitted to a serial interface through the use of plug-compatible converter modules. The serial interface reduces cable density, extends the interface distance, and is easily switched. The transmission media may be either coaxial cable or a fiber optic bundle. Additional economies are realized when the serial I/O system is integral with the main-frame equipment in which case the converter modules can be used on the peripheral equipment for compatibility between new and old systems. The transceiver modules are also applicable to regenerative type multisubscriber data buses and interconnect networks which are of paramount importance in the development of communications architecture for data processing systems.

Shown below is a top view of a dual bay AN/UYK-7. The left bay has 16 channels of parallel interfaces. The right bay has eight channels of low level serial interfaces and eight channels of parallel interfaces. Note that the white or black cables link an output channel to an input channel – used for factory testing. [lab]



THE EVOLUTION OF FIBER OPTIC SERIAL INTERFACES IN NAVAL TACTICAL DATA SYSTEMS

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ABSTRACT

Implementation of new interfaces in Naval Combat Systems is an evolutionary process. It is essential to provide a means of transition from the "old" to the "new" in order to retain interoperability among all elements of the system during their life cycle. This paper describes the evolution of fiber optic serial interfaces in U.S. Naval Tactical Data Systems (NTDS). Planned implementation of fiber optic interfaces in the new U.S. Navy Standard Shipboard Computers, AN/UYK-43 and 44, is discussed, as well as future requirements for higher-speed, bus-oriented interfaces which more fully utilize the wide bandwidth of fiber optic media and support the distributed system architectures of the future.

INTRODUCTION

The functional interface requirements for Naval Tactical Data Systems, as implemented in the U.S. Navy, are specified in MIL-STD-1397 [1]. This includes the requirements for interconnecting cables, interface circuits and cable connectors. This standard, in part, has served as the basis for the development of both interim and permanent shipboard data handling interface specifications for NATO Navies in cooperation with companies participating in Sub Group 6 of the NATO National Industrial Advisory Group.* NATO STANAGs (Standardization Agreements), developed by this group, include a general fiber optic interface standard, STANAG 4185 [2], and an application of this STANAG for a fiber optic interface as an extension to a specific serial interface for shipboard data handling systems, STANAG 4153 [3]. This is a 10 Mbs serial interface and has been specified as one of the input/output interfaces for the new U.S. Navy Standard Shipboard Computers, AN/UYK-43 and 44, being developed by the Computer Systems Division of Sperry Corporation.

*Current participating companies are as follows: Action 7S, CIMSA, TRT Electronique Serge Dassalt (France), AEG Telefunken and Elektro Spezial (Germany), ELSAG, FACE Standard and Selenia (Italy), Hollandse Signaalapparten (Netherlands), Kongsberg Vapenfabrikk (Norway), PLESSEY Radar and Ferranti Computer Systems (United Kingdom), Rockwell International, SEMCOR, and Sperry Corporation Computer Systems (United States).

The development and implementation of new interfaces in Naval Tactical Data Systems are evolutionary processes requiring careful consideration and evaluation of the impact the introduction of a new interface will have on the interoperability of the associated equipment. Typically, the life of the equipment involved, including enhancements, may exceed 20 years, and a gradual transition to new interfaces must take place with minimum modification to existing hardware. Accordingly, the benefits of the new interface must outweigh the additional costs for its implementation in new hardware, as well as retrofit of existing hardware to retain interoperability. This paper describes the gradual transition of Naval Tactical Data System interfaces from parallel, multi-wire, twisted, pair cable to serial, triaxial cable, to serial, fiber optic for point-to-point applications and ultimately to a high-speed, bus-oriented fiber optic interface applicable to the distributed system architectures of the future.

INTEROPERABILITY

As defined in MIL-STD-1397, Naval Tactical Data Systems hardware is interconnected, primarily through five interfaces which have evolved since the introduction of NTDS in combat systems in the early 60s. The characteristics of these interfaces are described in Table 1.

Typically, the hardware implementation of these interfaces is through interchangeable, interface cards which plug into the chassis of the input/output section of the computer or peripheral. Therefore, the interface type is an ordering option and can easily be changed in the field to upgrade or modify the system. All of the interfaces have a common protocol relative to internal communication with the host processor or peripheral, so that the interfaces can be upgraded without changing other sections of the hardware. Additionally, the system programming, except for throughput, is essentially independent of the interface type; therefore, higher-speed interfaces can replace slower-speed interfaces without change to system software. This is a key factor in effecting transition to higher-speed interfaces and in retaining interoperability of the basic hardware over the life of the system. Each new

TABLE 1. NTDS INTERFACES

Designation	Cable	Signal Level	Rate	Circuit Technology
Type A (NTDS slow)	Multi-wire twisted pair	0/-15V dc	41,667 words/sec	Discrete
Type B (NTDS fast)	Multi-wire twisted pair	0/-3V dc	250,000 words/sec	Discrete
Type C (ANEW)	Multi-wire twisted pair	0/3.5V dc	250,000 words/sec	TTL Logic
Type D Serial	Coaxial	±3.25 V Bipolar	10 Mbit/Sec	TTL Logic
Type E Serial	Triaxial	±.6 VDC Bipolar	10 Mbit/Sec	VLSI custom chips

interface has been introduced for one or more of the following reasons:

Type B NTDS Fast - To provide a higher throughput primarily for operation with disk memories.

Type C - ANEW - For airborne ASW systems to enable use of higher performance TTL Logic circuitry.

Type D - Serial - To extend the length of the interface to 1,000 feet through use of coaxial cable.

Type E - Serial - For U.S. Navy implementation of NATO STANAG 4153 for interoperability with NATO shipboard systems. This interface uses triaxial cable and low-level, transmission signals for improved EMI radiation characteristics. It also incorporates a burst mode or multi-word, transmission protocol for greater throughput.

STANAG 4153 Extension 2 (Fiber Optic) - This STANAG serves as the baseline specification for implementing a fiber optic serial interface in the AN/UYK-43 and 44. It is compatible with the protocol of the Type E electrical serial interface. The primary reasons for the use of fiber optic media for this interface are its immunity to EMP/EMI and its lack of radiation. It also is of lower density and immune to ground loop interference common in shipboard installations.

HARDWARE IMPLEMENTATION

New interfaces are initially introduced in the computer hardware elements of the system and used for intercomputer communications. Later, selected peripherals are modified for the new interface based on its projected life and overall usage in the system. An example of hardware that provides the transition from parallel to serial interfaces is the new Input/Output Adapter (IOA) for the AN/UYK-7 computer. The IOA is one of seven integral units of the computer and provides 16 input/output channels. A comparison of an AN/UYK-7 computer, configured with the current and new IOA adapter, is shown in a top view of the assembly in Figure 1. The IOA is mounted at the top of the computer and contains the connector receptacles for the I/O cables. This figure shows the current parallel IOA configuration on the left and the new configuration on the right, which provides a mix of parallel and serial channels. The new IOA adapter is shown in Figure 2 and in this unit is configured for eight serial and eight parallel channels. The interface cards are accessible from the top front of the unit. The circuitry for the serial input/output interface card is contained on one 4" x 9" card (Figure 3), whereas two cards are required for the parallel interface. A further example of the interconnect wiring savings of the serial interface is illustrated in Figure 4, which shows the wiring from the chassis to the connector panel. This is a plug-in, wiring harness (Figure 5), which means that the interface can be changed by plugging in the interface card(s) and the wiring harness. The bolt-circle pattern on the connector panel is common to both the serial triaxial and parallel multipin connectors.

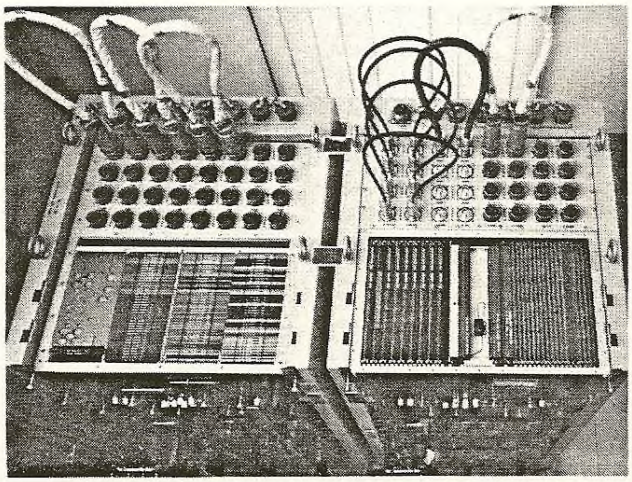

Figure 1. AN/UYK-7 Computer Top View - I/O Connector Panel

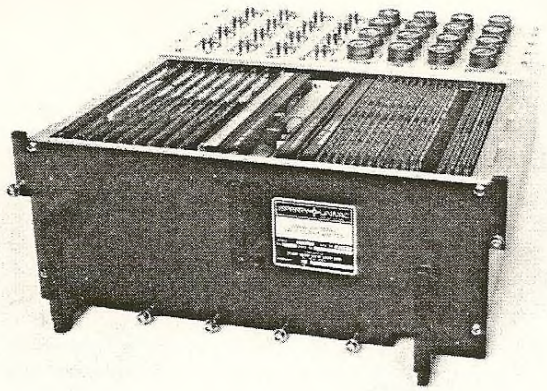

Figure 2. AN/UYK-7 Computer Low Level Serial Input/Output Adapter

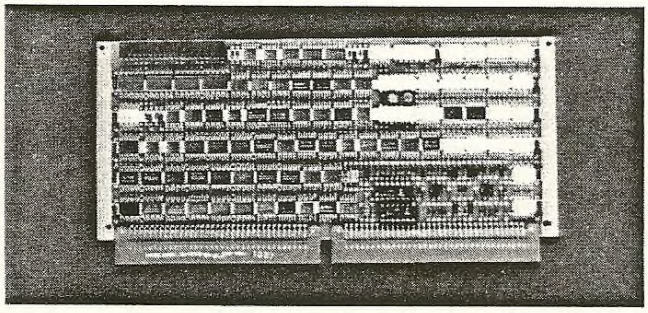

Figure 3. Low Level Serial I/O Card (4" x 9")

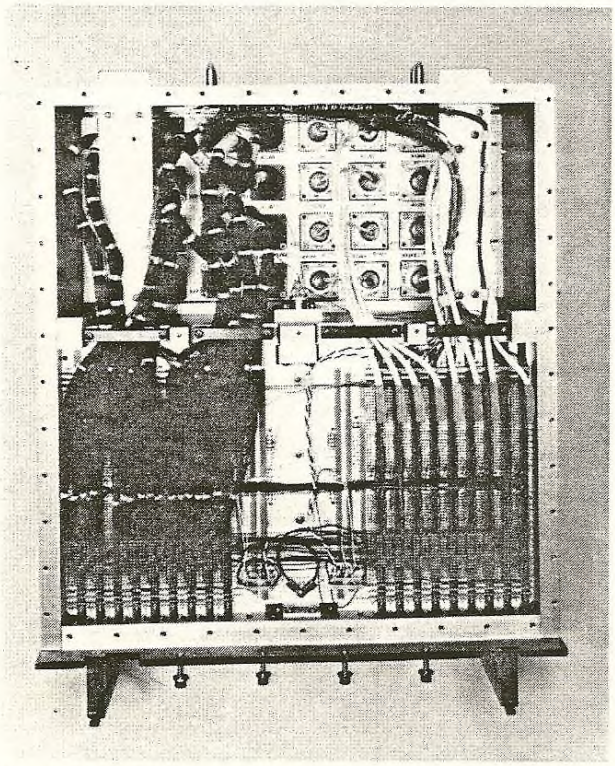

Figure 4. Low Level Serial I/O Adapter Interface Channel Wiring

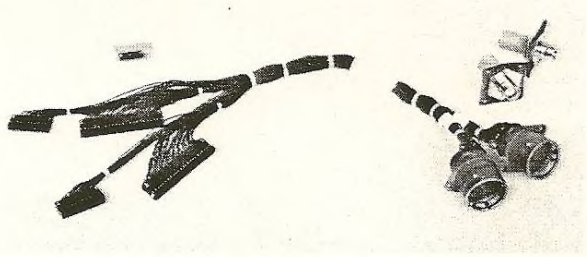

Figure 5. Low Level Serial I/O Adapter Internal Serial and Parallel Interface Cable Assemblies

FIBER OPTIC SERIAL INTERFACE

The U.S. Navy has elected to use fiber optics in shipboard combat systems, initially as a media alternative to triaxial cables as defined in the 10 Mbit serial interface, MIL-STD-1397, Type E. This gives the user the option to select either triaxial or fiber optic cable. The protocol is not affected by the medium selection.

The fiber optic interface as defined in STANAG 4153, Extension 2 specifies the optical characteristics of the signal at the input/output connector interface of the associated hardware (Figure 6). Specifically, a cone of emission (Figure 7) of the optical energy is defined at the connector interface for both the input and output signals, including the rise and fall time of the signal. Knowing the tolerances of the optical signal at the input and output interfaces, the designers are free to choose the type of fiber and cable assembly for their application. The primary functional constraints on fiber selection are its bandwidth, which must be sufficient to meet the signal rise/fall time requirements, and its attenuation, which, in combination with cable connector and other losses, must not exceed 20 dB for the link. Detailed specifications for the optical interface are contained in STANAG 4153, Extension 2.

HYBRID TRANSMITTER/RECEIVER MODULES

The Defense System's Division of Sperry Corporation Computer Systems has designed a product line of militarized, hybrid, electro-optic tranducers for both point-to-point and data bus applications up to 50 Megabaud (20 nanoseconds pulse width). The transmitter module (Figure 8) is common to all data rates, but the receivers are tailored to the specific system data rate. The units are contained in hermetically sealed packages with dimensions as shown in Figure 9, and are

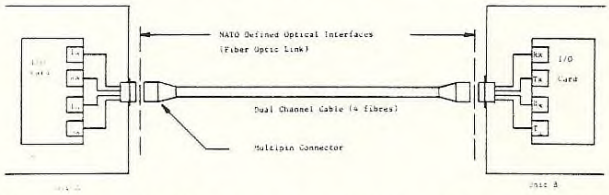

Figure 6. STANAG 4153 Fiber Optic Implementation

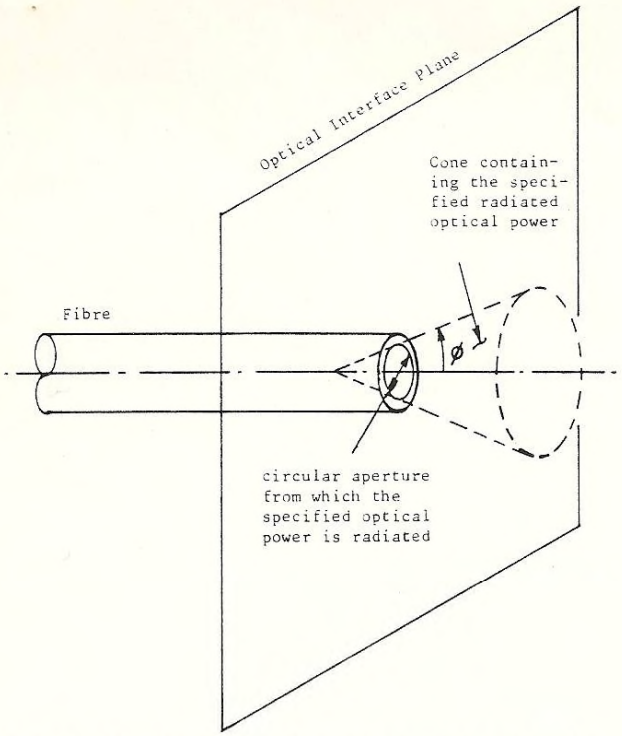

Figure 7. Optical Radiated Power Distributed Geometry

applicable to the STANAG 4153, Extension 2, serial interface.

The optical source for the transmitter module is an etched well Galium Aluminum Arsenide (Burrus) diode which emits optical power with a wavelength of peak radiance between 820 and 860 nanometers and a spectral bandwidth of less than or equal to 50 nanometers (half intensity). A

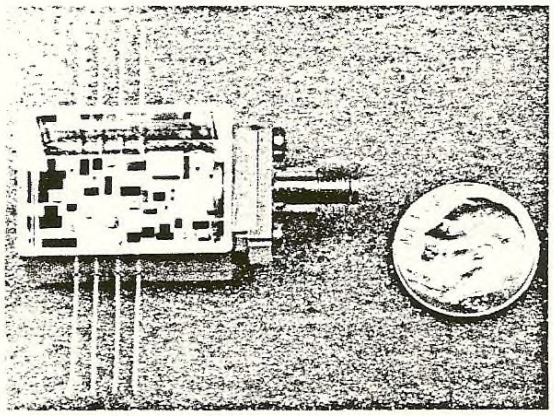

Figure 8. Hybrid Transmitter Module

glass, microsphere lens is cemented in the etched well, which provides an optical aperture (at the plane of the coupled fiber end) about 10 mils in diameter and with an 0.3 numeric aperture. Peak optical power launched in a step index fiber (100 micrometer core diameter, 0.25 N.A.) at maximum output power setting is 400 micro watts typical. The LED drive current is controlled by a temperature compensated current source that is

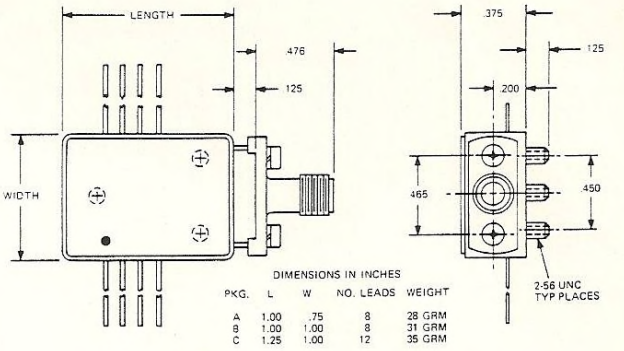

Figure 9. Fiber Optics Packages

altered by the LED junction temperature in a manner that maintains the LED radiant power output within a ten percent tolerance band over the operating temperature range. In addition, by grounding or opening three package pins in a binary, coded, octal sequence, the nominal current drive to the LED can be reduced from 100 percent to 25 percent in eight equal steps. This allows normalization of the optical output of a distribution of units or adjusting the output power level to suit the specific application. The performance specifications for the unit are summarized in Table 2 including its radiation hardening design limits.

STANAG 4153, Extension 2, specifies unipolar, baseband, Manchester modulation of the optical signal as derived from the three-level, biphase modulation of the baseline electrical STANAG. Compatibility of the link with both point-to-point and bus system applications is achieved by specifying that there should be no emission when the link is idle. The link protocol also specifies detection of the first bit of the frame, and since the intermessage gap can vary between 500 nanoseconds and one millisecond, a fixed-gain, data-bus-type, receiver design is required.

Sperry's line of receivers utilizes a hybrid preamplifier, which is scaleable to data rate, by changing R/C time constants for matched filter response to a given baud rate (bandwidth) with a linear relationship between baud rate and sensitivity. Specifically, in the hybrid microcircuit assembly, resistor scaling only is done; thereby, all resistors affecting bandwidth are scaled by the same factor. This is achieved without modification of the artwork or printing screens for the circuit substrates since the resistor values can be altered by control of the resistivity of the resistor pastes used to print the thick film substrate and trimming.

The functional block diagram for the data bus receiver is shown in Figure 10. The transimpedance amplifier is followed by a three-stage, non-linear, post amplifier which provides a gain of 600. The amplified differential signal is detected by a Schmitt trigger which provides output logic levels in both normal and complement forms. In this receiver, the intermessage gap is limited by the recovery of the tail of the differentiated waveform produced by the high-pass filter coupling the preamplifier to the postamplifier. When a

TABLE 2. TRANSMITTER SPECIFICATIONS

Launched Radiant Power Output (100 micron core fiber of 0.25 NA)	400 microwatts TYP.
Residual Radiant Power Output (no signal input)	0.1 microwatt MAX.
Emission Spectrum (wavelength)	820 to 860 nanometers
Bandwidth (Half amplitude)	50 nanometers
Optical Rise/Fall Time (20 to 80 percent amplitude)	10 nanoseconds max
Pulse Width Distortion	±10 nanoseconds
Jitter (20 Megabit input)	1 nanosecond max
Signal Input	TTL
Power Input	5 Volt, 250 ma, -12 Volt, 15 ma
Environment	MIL-E-5400 Class 2
Radiation Survivability Threshold Levels	
Total Gamma Dose	10^4 Rads
Neutron Fluence	10^{12} n/cm^2
Prompt Dose (Transient Upset)	10^8 RADS/SEC

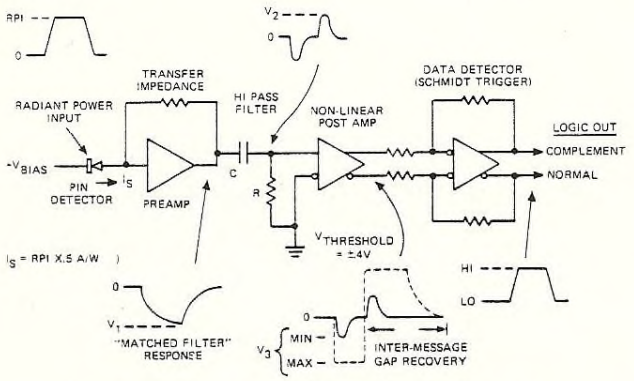

Figure 10. Receiver Block Diagram

message at a maximum optical signal level precedes a message at the minimum optical signal level, the tail of the differentiated, large signal must recover to a small level compared to the peak of the minimum signal. This recovery takes a maximum of ten times the width of the design baud width or five-bit periods if Manchester coding is used. For STANAG 4153, which requires a 20 Mbaud rate, this is 500 nanoseconds, which is the minimum intermessage gap of 500 nanoseconds and would permit use of the receiver in a data bus system.

The performance specifications for the module are summarized in Table 3, including its radiation hardening characteristics.

FIBER OPTIC/SERIAL INTERFACE DEMONSTRATION SYSTEMS

Extensive testing and demonstration of a new interface precede its introduction as a standard. In addition to gaining direct experience on the performance and hardware costs for the new interface, methods of transitioning current hardware to the new interface require evaluation to insure widespread usage of the new interface. In the case of STANAG 4153, the efficacy of converting existing parallel interfaces to serial interfaces through external parallel to serial I/O converters has been demonstrated in several production installations of switching systems at U.S. Navy land-based training and system integration test sites. Of concern is the ability of the system to tolerate the added delay of the conversion process in the interface protocol. If this delay is excessive, the use of external converters to adapt the parallel interface of peripheral equipment to the serial interface in new computers can limit the applications of the new serial interfaces.

One production switching system which provides confidence in the new serial interface standard is the AN/USQ-67 Centrally Controlled Interconnection System installation at the Combat System Maintenance Training Facility at Mare Island Naval Shipyard, Vallejo, California. This system provides for the interconnection of 640 parallel interfaces over a serial transmission system operating at 25 Mbaud. External converters are used for serialization and plugged directly into the I/O receptacles of the computer and peripheral hardware. The transmission system demonstrates the performance of a low voltage (less than 0.5V) transmission system using triaxial cable. A low voltage transmission system using triaxial cable is specified for STANAG 4153, and its selection is, inpart, based on the performance of this system. In addition, it demonstrates that

TABLE 3. RECEIVER SPECIFICATIONS

Input Sensitivity	250 nanowatts
Dynamic Range	23 dB
Input/Optical Rise/Fall Time	20 nanoseconds max (10-90 percent)
Data Rate	20 Megabaud
Bit Error Rate	$<10^{-9}$ at 250 nanowatts input
Signal Output	TTL
Power Input	5V, 30 ma, -12V, 30 ma, 28V, 100 nanoamps
Environment	MIL-E-5400 CLASS 2
Radiation Survivability Threshold Levels	
Total Gamma Dose	10^4 RADS
Neutron Fluence	10^{12} n/cm^2
Prompt Dose (transient upset)	10^5 RADS/SEC

the 25 Mbaud, serial, transmission rate is sufficient to interconnect most of the NTDS hardware suite without software changes. Thus, implementation of the serial interface within the I/O section of the hardware can proceed with high confidence that all NTDS equipment can be interconnected with the new interface.

The converters used in the AN/USQ-67 system are constructed of hybrid circuits mounted within a package envelope that allows direct connection to the computer and peripheral hardware. These converters are also used to evaluate serial transmission over fiber optic cable. The electrical, transceiver hybrid has been replaced with a fiber optic transmitter/receiver module that attaches directly to the cable connector end of the converter case. Several of these fiber optic converter sets (Figure 11) have been tested at land-based test sites and on shipboard installations involving NTDS hardware, again demonstrating the applicability of fiber optic transmission systems.

CUSTOM VLSI INTERFACE CIRCUIT DESIGN

Implementation of the NATO STANAG 4153 serial interface in shipboard hardware has evolved from initial installations which used printed, circuit cards with discrete/MSI components to the use of custom VLSI circuits in chip carriers mounted on ceramic cards (SEM Format B). The VLSI implementation consists of three chips which perform the interface circuit functions shown in the block diagram of Figure 12. The STANAG 4153 protocol for the serial input and output control/data functions are provided by two gate arrays, which in combination with a third SNERT chip (Serial Nato Encoder/Decoder Transceiver), provide the two independent functions required for one, full, duplex, serial, I/O channel. The encoder/decoder portion of the SNERT chip accepts TTL clock timing, NRZ data and driver enable signals from the output control/data gate array and generates the Manchester II code signal for serial baseband transmission at ten megabits per second. Similarly, the receiver/decode portion of the chip receives the Manchester II code signal from the triaxial cable, decodes the serial data, clocks information and provides TTL compatible signals to the input control/data gate array. Coupling to and from the triaxial cable is through an external transformer.

An additional feature of the SNERT chip is the capability to loop back data and control signals from the input and output gate arrays which allow data sent from a computer output channel to be looped back internally and received as input data on the computer input channel. This provides I/O channel test capability at the system level without disconnecting the I/O cables and reconnecting a jumper cable for tests.

The SNERT chip is shown in Figure 13. The die size is 150 mils square and is mounted in a one inch square, 64 leadless chip, carrier package. This process is Schottky Transistor Logic. The chip contains 17,000 transistors and dissipates 1.3 watts compared to six watts for the predecessor, discrete, circuit design.

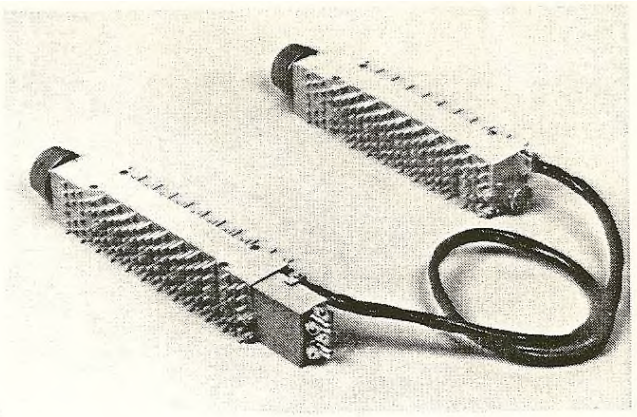

Figure 11. Fiber Optic Serial I/O Converter Set

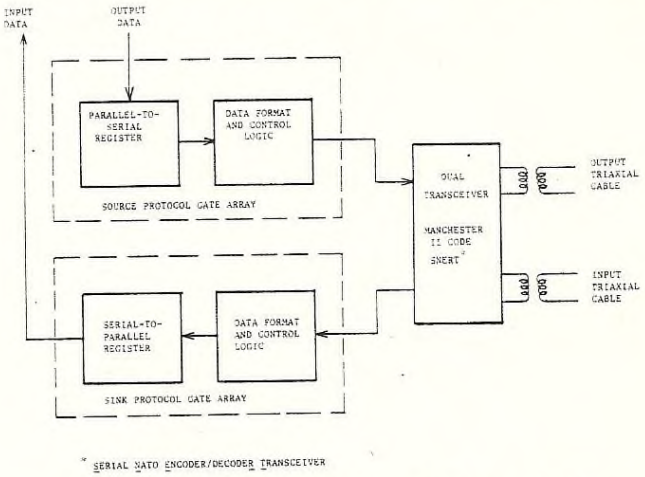

Figure 12. Serial I/O Block Diagram (Chip Implementation)

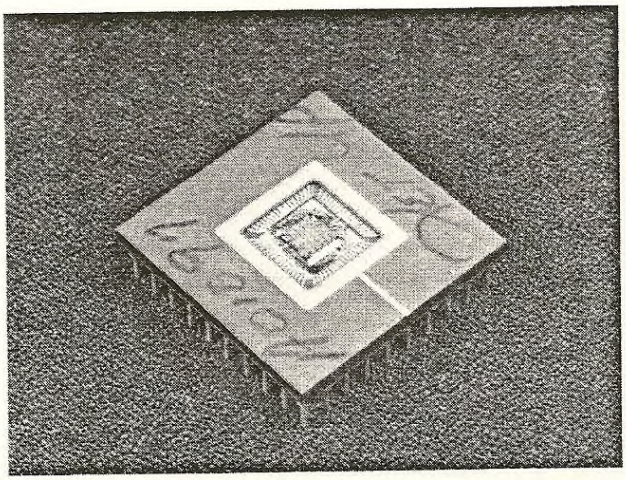

Figure 13. Serial Nato Encoder/Decoder Transceiver (SNERT Chip)

These three VLSI circuits are the principal components used for both the electrical and fiber optic media implementation of the STANAG 4153 serial interface in the AN/UYK-44 computer. The

SNERT chip is also used in the AN/UYK-43 serial interface card. For electrical media, the SNERT chip interfaces directly with the cable through coupling transformers. For fiber optical cable, the SNERT chip provides the signals for driving the optical transmitter and receiver and processes signals from the optical receiver. Additional logic circuitry is required to provide conversion of the three-level, electrical, Manchester code generated within the SNERT chip to the two-level, unipolar, baseband signal required for optical transmission. In practice this circuitry affects only the first and the last bits in a transmission since the two codes are identical for intervening bits. The STANAG 4153 protocol specifies that the first bit is always a "one," so the fiber optic link is driven from the quiescent to a high state on the first transition, which is compatible with the three-level code. The last bit in a transmission may be either a "one" or a "zero". Since a "zero" is recoginized in a three-level, Manchester code by a transition from a low to a high state at the mid-bit point, it is necessary for the unipolar logic to return the link to the low state at the end of the transmission (recognized by the absence of further transitions). Typically this results in the receive message being delayed two to three bits for detection of the end of the message. This logic circuitry and the optical components are colocated on the I/O card or external to the card, depending upon the card size and computer configurations.

AN/UYK-43 SERIAL I/O INTERFACE IMPLEMENTATION

The AN/UYK-43 standard shipboard computer is built in two configurations (Figure 14). One configuration has 24 I/O channels in which the I/O cable connector panel is on the top of the bottom section of the computer (Figure 15), and the other configuration has 64 channels in which the I/O connectors are on the backside of the computer. Both configurations provide any mix of parallel or serial channels on an individual channel basis as compared to the four-channel grouping of the predecessor AN/UYK-7 computer.

The method of configuring the I/O channels is similar to that implemented in the new AN/UYK-7 Input/Output Adapter. The interface circuitry for each channel is contained on a 7" x 12" printed circuit card which plugs into the I/O section of the computer. An individually, replaceable, cable harness and connector assembly are used to provide the signal path between the I/O chassis and the I/O connector panel. Printed-circuit flexible cable is used for the parallel interfaces and coaxial cable for the serial interfaces.

For the fiber optic serial interface, the optical hybrid transmitter and receiver modules (two sets) are mounted on the I/O PC card and a four-fiber cable assembly consisting of four, co-bundled, individual, fiber optic pigtail cables is used to route the optical signals from the PC card to a four-pin connector on the I/O connector panel. The profile (height) of the fiber optic hybrid packages has been reduced from 3/8" to 1/4" to permit direct mounting of the modules on the PC cards.

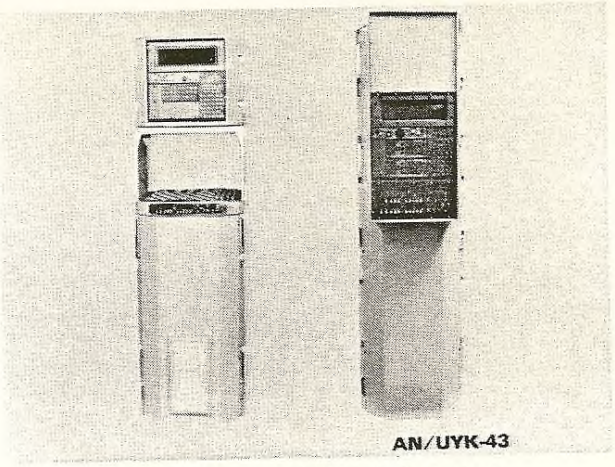

Figure 14. AN/UYK-43 Computer

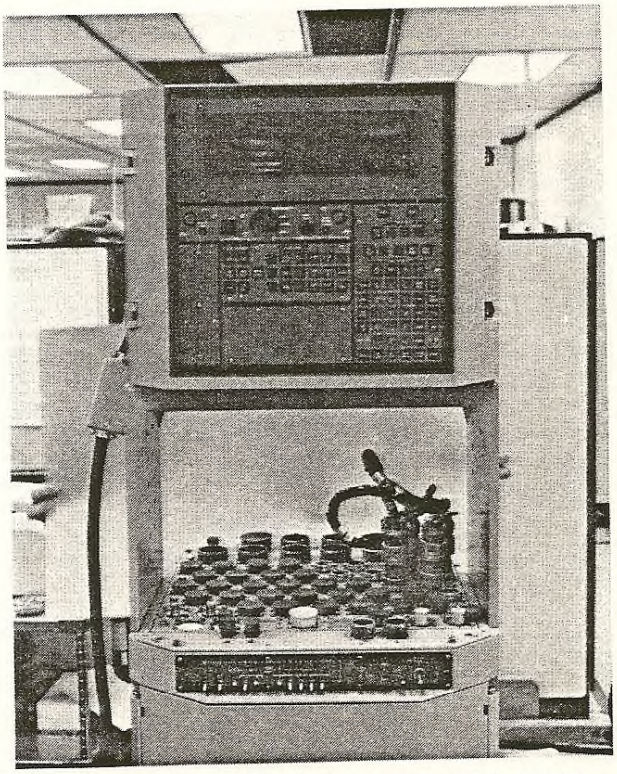

Figure 15. I/O Connector Panel (AN/UYK-43)

AN/UYK-44 SERIAL I/O INTERFACE IMPLEMENTATION

The AN/UYK-44 computer (Figure 16) contains 16 I/O channels which may be configured to any mix of standard parallel or serial channels with a modularity of two channels for each type. The I/O connectors are mounted in two channel groups on the back of the computer (Figure 17) and are accessible/removable from the front of the computer. These modules (Figure 18) contain the I/O connectors and include transorbs on each pin for Electro Magnetic Pulse (EMP) hardening.

The circuitry for the serial interface is contained on one, two-sided, Format B, SEM cards (2 x 5 3/4 inches) in which the SNERT chip and

associated discrete components (delay lines, transformers, filters, etc.) are mounted on one side and the two source and sink protocol gate arrays and associated discrete buffer circuits on the other. A second control card is also required for each channel which provides the interface circuits to the internal parallel bus system. A comparison of the relative size of the I/O interface cards for the AN/UYK-44, with those of the predecessor AN/UYK-20 computer, is shown in Figure 19.

For the fiber optic implementation of the interface, the I/O connector module (Figure 20) is modified to incorporate the optical and receiver hybrids (four sets), which are required to provide two I/O channels. These hybrids are mounted on PC cards in the back of the I/O connector module in place of the cards containing the EMP transorbs. In addition the front of the module is extended to accommodate two, four-pin, fiber optic connectors and provide space for routing the individual fibers to the single-fiber connectors on the hybrid modules. Note that with reference to the STANAG 4153 fiber optic interface diagram (Figure 6), a four-fiber cable provides both the input and output channels of the interface so that only two fiber optic connectors are required on the connector I/O module for fiber optic media, as compared to four for the electrical interfaces. The fiber optic I/O connector module interfaces internally with the electrical serial I/O cables within the I/O section of the chassis. Power is routed directly to the module for supplying power to the optical components within the module.

HIGHER-SPEED BUS-ORIENTED FIBER OPTIC INTERFACE

Current implementations of the fiber optic extension to the STANAG 4153, 10 Mbs, serial interface support fiber optic interconnect applications where compatibility with the existing serial I/O protocol is required. In this case, the fiber optic media provides immunity to EMP interference and group loops, does not radiate, is smaller and lighter than electrical cable and can easily provide interface distances greater than the 300 meters of the electrical interface. This interface is a good first step in the evolution of fiber optic interfaces in naval tactical data systems.

Much consideration is now being given and designs are in process for embedded system applications of the AN/UYK-44 computer, particularly in multiple computer distributed systems interconnected by one or more bus system. To provide the required throughput and access time for these systems, a much higher data transfer rate than the 10 Mbs provided by the current serial interface standard is needed. It is apparent that a standard bus interface operating in the 40 to 50 Mbs range and utilizing the wide bandwidth and interference immunity attributes of fiber optics serves this need. Such an interface serves both point-to-point and bus system applications for interconnecting Combat Systems and is designed to interface directly with the internal bus system of the host computer. Through the use of the VLSI circuit technology, the card space for imple-

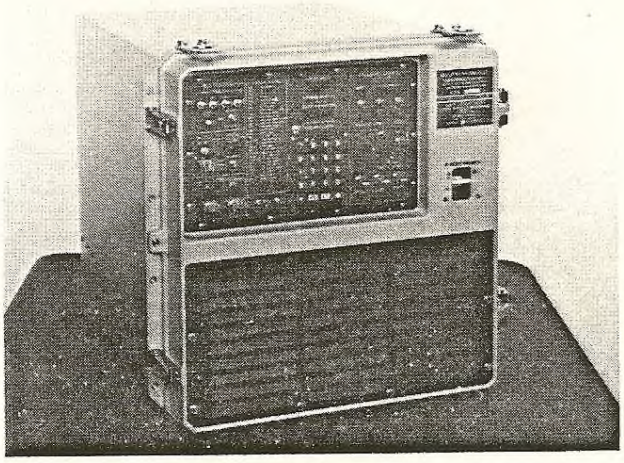

Figure 16. AN/UYK-44 Computer

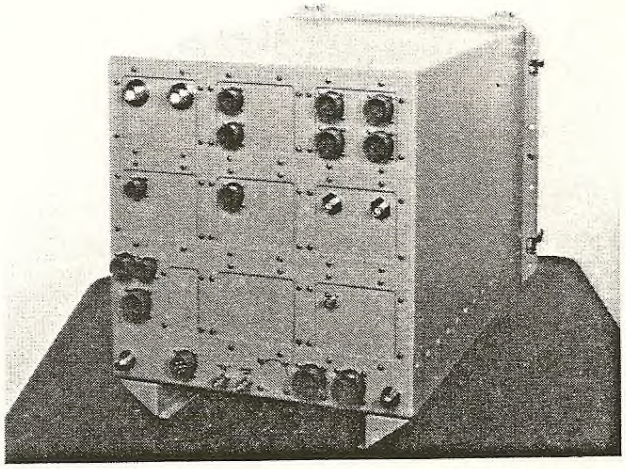

Figure 17. I/O Connector Panel (AN/UYK-44)

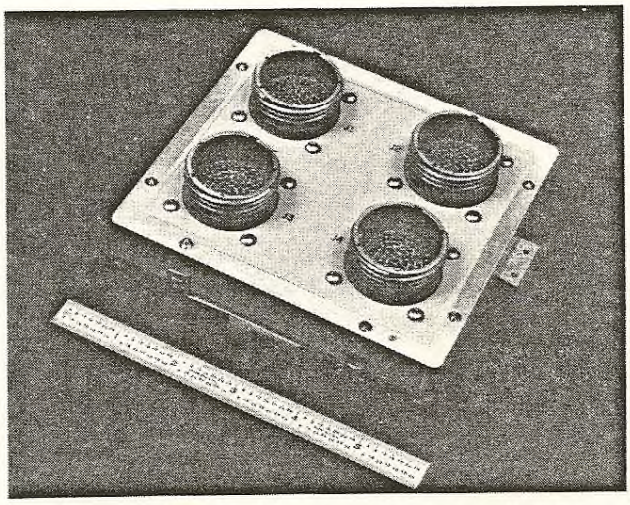

Figure 18. I/O Connector 2 Channel Module (Parallel Interface)

ference immunity attributes of fiber optics serves this need. Such an interface serves both point-to-point and bus system applications for interconnecting Combat Systems and is designed to

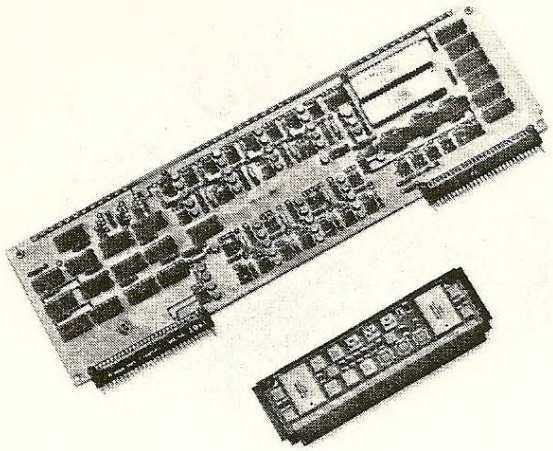

Figure 19. UYK-20/UYK-44 Card Size Comparison

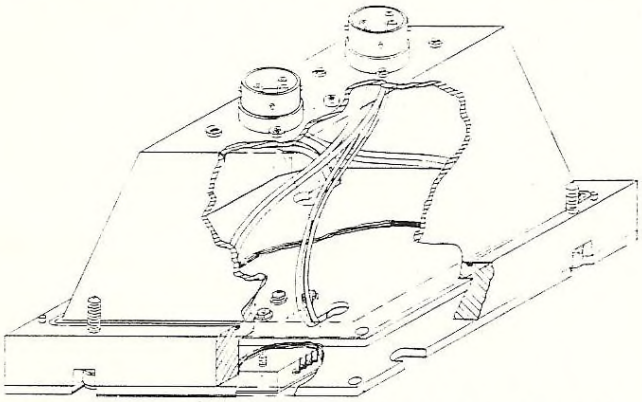

Figure 20. Fiber Optic Adapter Module (Two I/O Channels)

menting this interface in the AN/UYK-44 is comparable to that required for a two-channel I/O group (4 SEM B cards). Thus, the system integrator would add an additional high-speed interconnect option to the current mix of parallel and serial interfaces.

Several bus systems have been developed for interconnecting Naval Combat Systems in which the bus terminals are external to the combat system hardware and interface through standard I/O interfaces (the Canadian Navy's Shipboard Integrated Processor and Display System,* SHINPADS [4], and the U.S. Navy's Shipboard Data Multiplex System, SDMS [5] are examples). While these systems are effective in interconnecting current hardware in a distributed system application, they do not provide the economy or improvement in performance that can be realized by embedding the bus interface within the host hardware. Embedded bus interfaces eliminate the link between the host user and the bus terminal, thus eliminating the cost of this interface hardware, as well as the circuit delays in processing the data through the interface. In fact, in the production implementation of the SHINPADS bus system in the Canadian Patrol Frigate, all the AN/UYK-502 processors used in the combat system incorporate an embedded bus interface in which the bus terminal (node) interfaces directly with the internal bus system of the processor.

The above serves to illustrate the evolutionary process in improving the interconnect systems for Naval Tactical Data Systems and emphasizes the need for standardizing a high-speed, embedded, bus interface to prevent the proliferation of system-unique data buses which will occur as distributed system architectures are implemented by different system integration contractors.

SUMMARY

Serial I/O interfaces are gradually replacing the multi-wire, twisted pair parallel interfaces as the primary means of interconnecting elements of Naval Tactical Data Systems. The NATO STANAG 4153, 10 Mbs, serial interface is available in both electrical (triaxial) and fiber optic cable as the transmission medium and is being implemented in the AN/UYK-43 and 44 standard shipboard computers. The I/O section of these computers are designed to easily accommodate changes in the interface type, as well as the transition to new interfaces which evolve during the life of the equipment. Development of a standard high-speed fiber optic bus interface is recommended to support the distributed system architectures of the future.

References:

[1] MIL-STD-1397: Input/Output Interfaces, Standard, Digital Data, Naval Systems.

[2] NATO STANAG 4185: Standard Specification for Fiber Optic Interface Parameters to be Used in Naval Systems Digital Links.

[3] NATO STANAG 4153: Standard Specification for an Asynchronous Serial Data Interface for Point-to-Point Connections and for Connections to Data Networks in NATO Naval Systems.

[4] SHINPADS - A New Ship Integration Concept. CDR James F. Carruthers, Canadian Forces, Naval Engineers Journal, April 1979.

[5] Shipboard Data Multiplex Systems (SDMS) - A New Design for Lower Ship Cost and Improved Flexibility. Dr. Noybert T. Bold, Martin Wapner & Luther Blackwell Naval Engineers Journal, April 1976.

* Canadian Forces Trademark