# UNIVAC DIGITAL CIRCUIT MODULES

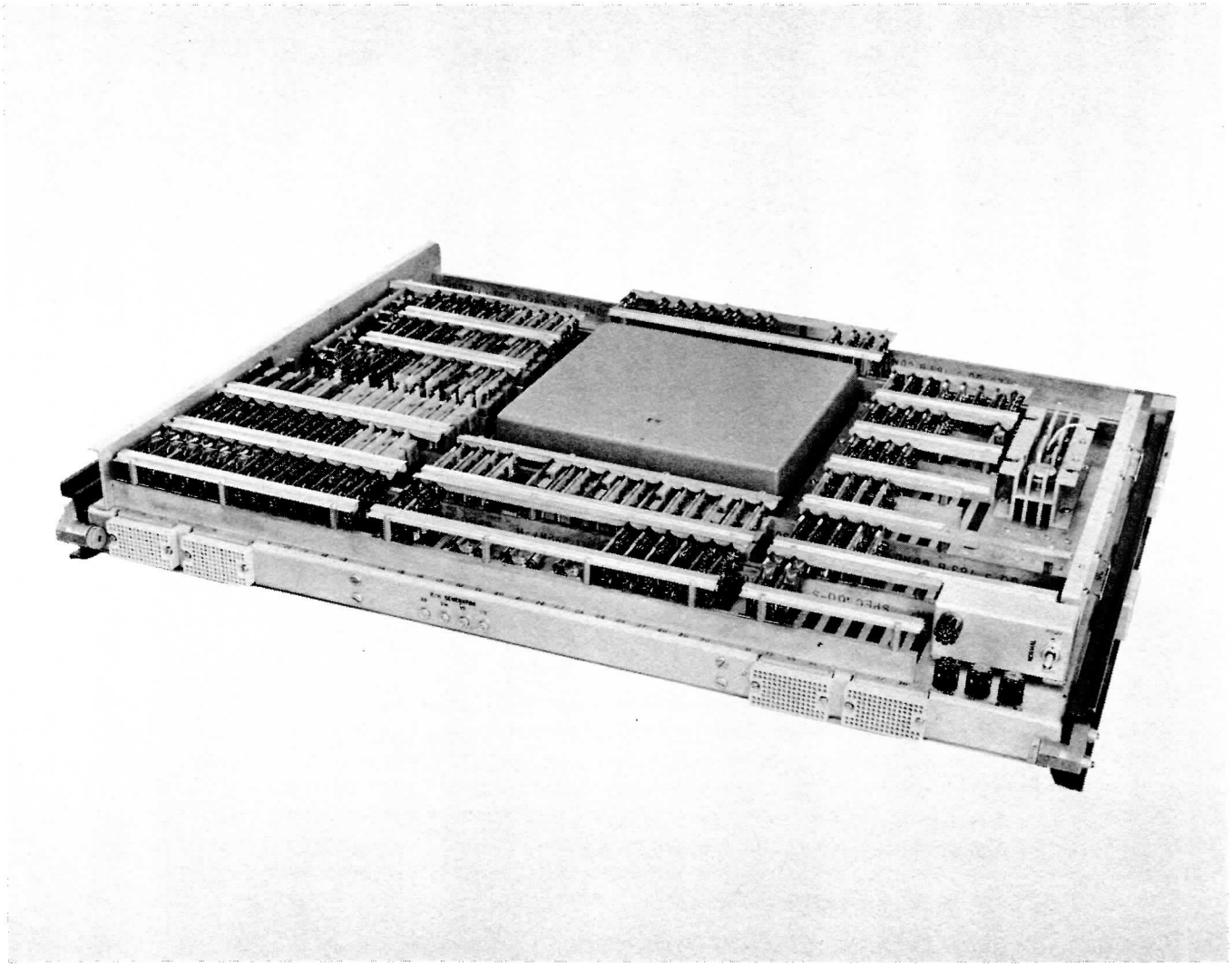
## FOR MILITARY APPLICATIONS

....DATA PROCESSING EQUIPMENT

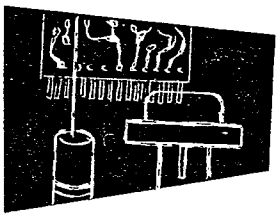
...LOGICAL CONTROL SYSTEMS

..DIGITAL SYSTEMS

UNIVAC
DIVISION OF SPERRY RAND CORPORATION
DEFENSE OPERATIONS • UNIVAC PARK • ST. PAUL, MINN.



Typical Computer Logic Tray with Covered Memory Stack



# GENERAL INFORMATION

## INTRODUCTION

The series of UNIVAC digital circuit modules described in this brochure consist of two basic logic elements: (1) AND/OR, and (2) AND. A choice between these two types of logic elements affords very efficient solutions to logical configurations. This approach simplifies maximum repetition rate considerations since the number of logic levels required for a given logic system can be kept to a minimum. The output impedances of these circuits are identical. This compatibility between circuits makes functional block diagram design problems easier and mechanized design techniques simpler.

## RELIABILITY

All semiconductor devices utilized on these modules were carefully selected for reliable long life and resistance to adverse and varying environments. These devices are either military types or have been approved for use by the Bureau of Ships. An attempt has been made to use standard, uniform devices without sacrificing performance or reliability. For example, 83 percent of the total transistors are of one basic family (i.e., PNP germanium mesa transistors), and 90 percent of all diodes are of one germanium type. Failure rates based on 150,000 hours of computer operation indicate a transistor failure rate of $5.21 \times 10^{-5}$ percent per thousand hours.

Quality is maintained by vendor surveillance, rigid quality assurance provisions of environmental testing, and failure analysis of failed or suspected parts, with feedback to vendors for product improvement.

Passive components, used sparingly, consist primarily of carbon composition resistors, glass capacitors for critical applications, and solid tantalum capacitors, all procured to military specifications. Ceramic capacitors are of the highest quality and meet or exceed military requirements.

Failure rates based on 150,000 hours of computer operation are as follows:

| | |
|---|---|
| Resistors | $.28 \times 10^{-5}$ percent per thousand hours |
| Capacitors | $1.77 \times 10^{-5}$ percent per thousand hours. |

In typical military computer applications, UNIVAC digital circuit modules have a card failure rate of $2.68 \times 10^{-7}$ cards per hour, or 0.268 card failures per million hours and continuing experience indicates that the failure rate is constantly improving.

## QUALITY

All digital circuit modules are built to meet shipboard requirements while confined within a cabinet enclosure. These requirements, listed in UNIVAC specification GS-5000, include:

MIL-E-16400 (Navy): Electronic Equipment, Ship and Shore

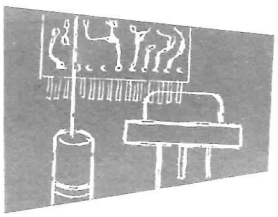
QQ-S-571: Solder, Soft

MIL-STD-275: Printed Wiring, Electronic Equipment

Soldering techniques and resultant quality are required to meet or exceed the exacting criteria of MIL-STD-440 and MIL-S-6872. Failure rates of solder joints are approximately 0.4 failures per million hours of machine operation in large, complex computer systems.

Manufacturing assembly operations also include routine, alert evaluation of lot quality. Manufacturing has the capability for 100-percent testing of selected lots when required. Each technique and quality parameter are carefully documented. Final operation consists of exercising each card to determine its conformance with functional requirements before it is finally accepted.

Environmental evaluation includes elevated as well as depressed operating ambients and operation after exposure to shock and vibration.

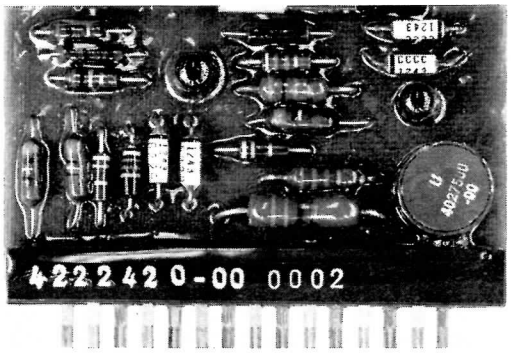


## COMPATIBILITY

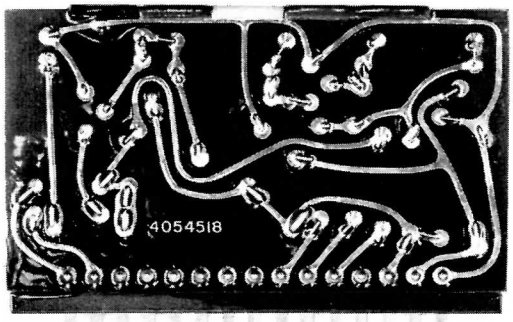
The UNIVAC family of digital circuit modules includes several that are capable of interfacing with other types of digital equipment such as tape readers, high-speed printers, and magnetic tape units. Also, digital circuit modules of any one type are interchangeable in any position when used in accordance with the specified design rules. Because of this flexibility, the design and assembly of integrated systems are greatly simplified.

## PHYSICAL DESCRIPTION

With few exceptions, digital circuit modules can satisfy all the circuit requirements of computers and peripheral equipment. Each card measures approximately 2-5/8 inches long by 1-15/16 inches wide, and accommodates from one to five logic elements. Each card has a multiple connector made up of 15 contacts which are numbered from 1 to 15. Eleven contacts provide connections for input or output signals, and four contacts connect the card to d-c power supplies and machine ground.




The 15-pin male connector body material is Diallyl Phthalate, type SDGF, per MIL-M-14 or GDI 30 F per MIL-M-19833. Contacts are brass (per QQ-B-626), and the contact finish is electroplated tin over nickel plate, or gold plate over nickel plate.




Minimum spacing from centerline to centerline is .450 inches between modules or connectors. Circuit modules are available with gold or tin alloy connectors. Part numbers for the gold or tin alloy are on the data sheets.

Dip-soldered, etched circuits on epoxy glass laminate, copper-clad cards are utilized for maximum durability, ensuring optimum performance under adverse conditions. Assembled cards are epoxy dipped to provide additional mechanical strength and increased resistance to environments.

The digital circuit modules were designed in compliance with MIL-275B.

## MATING CONNECTORS (Female Receptacles)

The mating female connectors for these modules can be obtained in several forms from many manufacturers. If the user selects modules with gold-plated pins, then he must also select receptacles with gold-plated contacts. Similarly, if modules with solder-plated pins are chosen, receptacles with solder-plated contacts must be chosen. In either case, taper pin or wire-wrap terminals can be chosen. A list of vendors and the appropriate vendor part number follows:

Connector, female, gold-plated contacts, taper-pin terminals

| | |
|---|---|
| Amphenol | Part No. 143-825 |
| Burndy Corp. | Part No. 8215-P1 |
| National Connector Co. | Part No. 12C-32A-45 |

Connector, female, solder-plated contacts, taper-pin terminals (the solder-plated connector is a special variation of the gold-plated version)

| | |
|---|---|
| Amphenol | Part No. 143-825 |
| Burndy | Part No. 8215-P1 |
| National Connector Co. | Part No. 12C-32A-45 |

Connector, female, gold-plated contacts, wire-wrap terminals

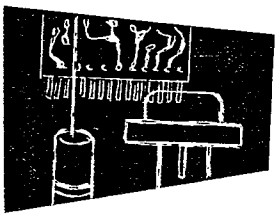
| | |
|---|---|
| Burndy | Part No. EL 9295 (without ground clip)<br>Part No. EL 9297 (with ground clip) |
| Berg Electronic Inc. | Part No. 50146-2 (without ground clip)<br>Part No. 50146-3 (with ground clip) |

Connector, female, solder-plated contacts, wire-wrap terminals

| | |
|---|---|
| Burndy | Part No. EL 9294 (without ground clip)<br>Part No. EL 9296 (with ground clip) |
| Berg Electronic Inc. | Part No. 50146 (without ground clip)<br>Part No. 50146-1 (with ground clip) |

## ELECTRICAL GROUND RULES

Ground rules for interconnecting wires and circuit fan-out are given on the data sheets associated with each logic module. The maximum switching time for each printed circuit is also shown on these data sheets.



General rules for the interconnecting wires are as follows:

(1) The maximum total wire length from any output is 60 inches. The three output pins from a driver circuit, 4222011, are considered one output;

(2) Wires may run parallel to each other for a maximum of six inches;

(3) Wires should be loosely bound to minimize coupling.

## Pin Allocation

Pins 1 through 4 on all assemblies are standard voltage pins. Standard pin allocations are as follows:

Pin 1 - ground

Pin 2 - + 15 volts, ± 10 percent

Pin 3 - -15 volts, ± 10 percent

Pin 4 - -4.5 volts, ± 10 percent

In addition to the ± 10 percent tolerance on individual voltages, the three voltage differences must track within 6 percent (i.e. when the + 15 v source decreases, the - 15 v source must also decrease.) Nominal voltage excursions for all assemblies are called out on the data sheets. These excursions will be within the above tolerances.

## DEFINITIONS

*Turn-on* time for logic circuits is defined as the time duration between the start of transition time of the input pulse and the -0.4-volt point of the output pulse.

*Turn-off time* is defined as the time duration between the start of the transition time of the input pulse and the -3.0-volt level of the output pulse.

*Fall time* is measured to the -3.0-volt level because the input diodes reverse at some voltage level near -3. A voltage level more negative than -4.5 volts may be used at the input to a logic circuit for special applications if the switching speeds are slow and the voltage swing is not excessive.

*Logical* "0" voltage level is actually between 0 and -0.4 volt. The *logical* "1" voltage level is dependent on the -4.5 volts supply voltage tolerances. This supply should be -4.5 vdc ±10% and ripple free.

## SYMBOLS

*Symbols* for the logic circuits are in accordance with MIL-STD-806B (modified). The symbols given on the individual data sheets are not necessarily the proper symbols for the circuit application: the symbol is determined by title only.

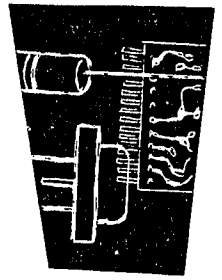
## TYPICAL APPLICATION

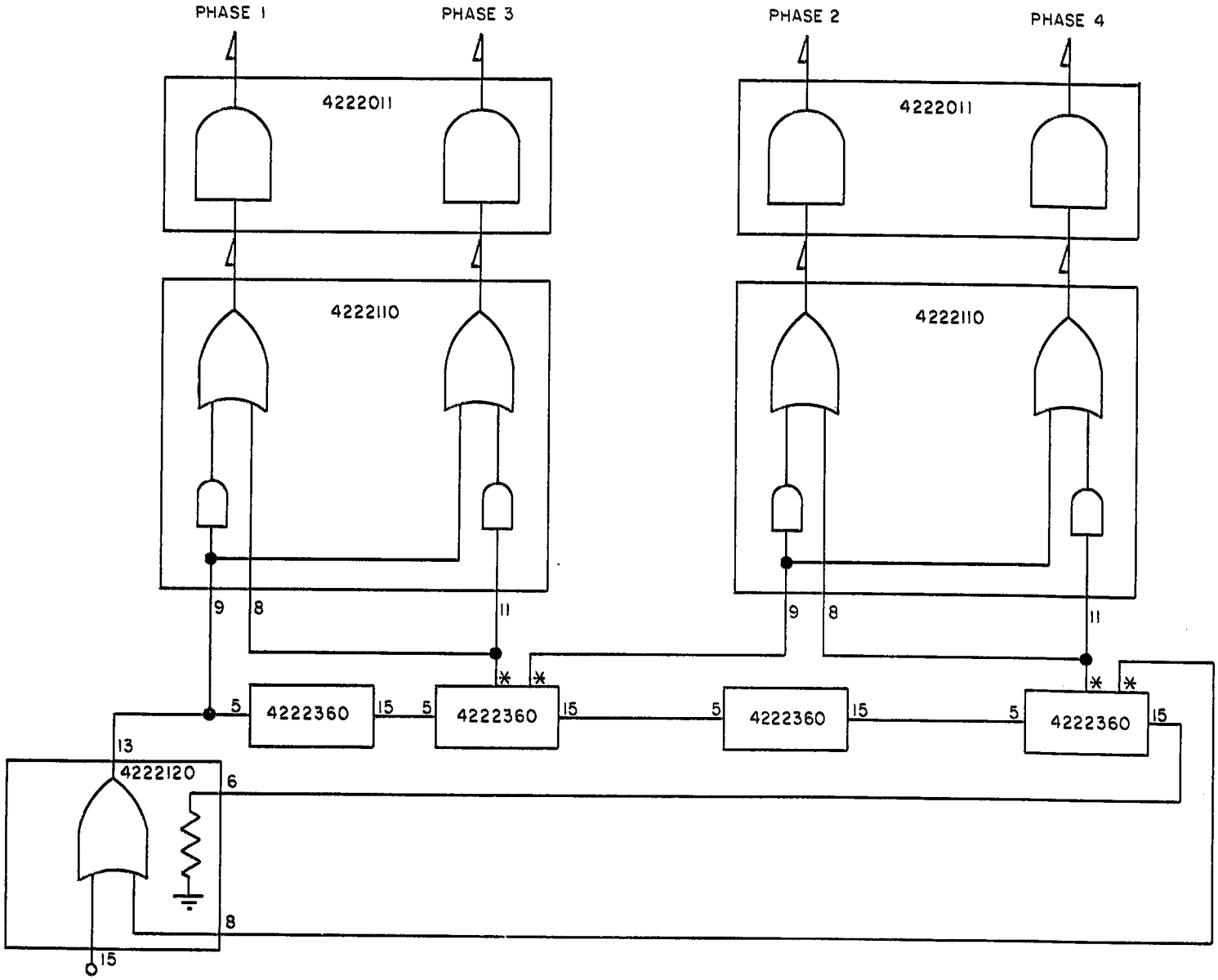
A typical circuit for a 4-phase master clock is shown on the following page. This clock is composed of a delay line driver card, four 0.1 microsecond delay lines, two clock timing driver amplifiers, and four logic driver circuits.

The output from the delay line driver card, 4222120, is connected to the input of four delay lines in series, type 4222360. The output of the last delay line in the string is terminated into the terminating resistor on the 4222120 assembly.

The clock timing driver amplifiers, 4222110, are connected to the delay lines as shown in the schematic to form the individual clock phases. There is a time delay between adjacent clock phases to prevent overlap of adjacent phases. Each phase can be adjusted for pulse width by shifting taps on the delay line. The over-all cycle time is adjusted by shifting delay line taps on the input to the 4222120 assembly. The cycle time for this example is about 670 nanoseconds. Each phase is approximately 167 nanoseconds.

Pin 15 on the delay line driver card, 4222120, may be used for phase stepping the clock, stopping the clock, or other purposes.



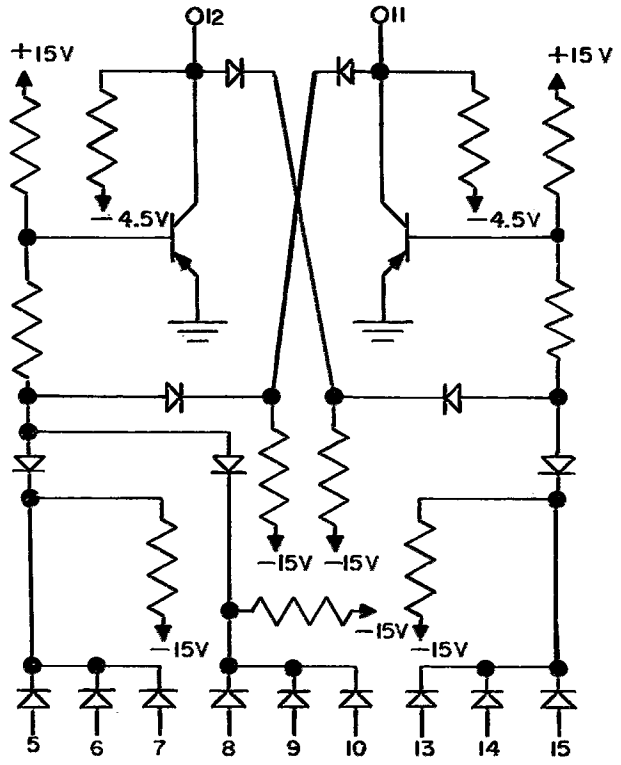



* Pin numbers will change due to inherent delays of phase generators and the delay line driver.

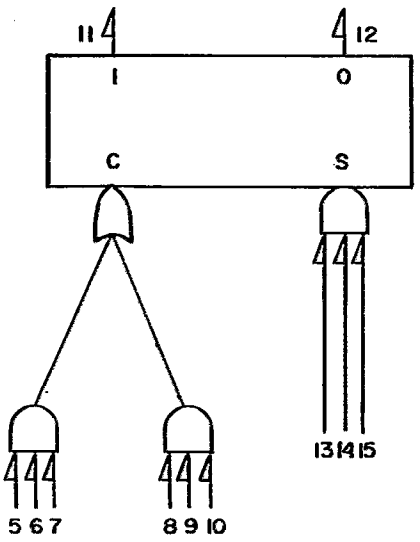
FLIP-FLOP (33-3)

4222020 Gold

7002020 Tin




SIMPLIFIED SCHEMATIC




LOGIC SYMBOL

## DESIGN DESCRIPTION

This circuit operates with input pulses that have nominal positive excursions of 0 vdc and nominal negative excursions of -4.5 vdc. The excursions of the output voltage pulses are the same as those given for the input pulses. The maximum input current required is 7.1 ma at 0 vdc input.

The circuit can drive four ANDs plus one indicator driver, or four AND/ORs plus one indicator driver.

The maximum circuit turn on and turn off time is 50 and 60 nanoseconds respectively under the conditions stated in the General Information section. The time through the flip-flop is the time required through two logic circuits.

| POWER | | | | |
|---|---|---|---|---|
| Pin | 1 | 2 | 3 | 4 |
| Voltage | Gnd | 15 | -15 | -4.5 |
| MW | | 64 | 470 | 43 |

## LOGIC DESCRIPTION

The right side of the flip-flop symbol is referred to as the "set" side, and the left as the "clear" side.

When the AND on the right side has all logical "1"s as inputs, the output on the right side is a logical "1" and the output on the left side is a logical "0". When one of the ANDs on the left side has all "1"s inputs, the output on the left side is a "1" and on the right side the output is a "0".

NOTE: The input configuration can be reversed so that the multiple-input inverter functions as the clear-side inverter.

| LOGIC | | | |
|---|---|---|---|
| INPUT | | OUTPUT | |
| "0" | "1" | "0" | "1" |
| 0v | -4.5v | 0v | -4.5v |