NORMAL k DESIGNATOR

k	READ		STORE		REPLACE			JUMP	
	MN.	Origin	MN.	Dest.	MN.	Origin	Dest.	MN.	Jump to Modulo 2^{18}
0	'blank'	sy + Bb	QR	Q	'not used'	–	–	'blank'	sy + Bb
1	L	$\underline{Y}_L$	L	Y_L	L	$\underline{Y}_L$	Y_L	L	$\underline{Y}_L$
2	U	$\underline{Y}_U$	U	Y_U	U	$\underline{Y}_U$	Y_U	U	$\underline{Y}_U$
3	W	$\underline{Y}$	W	Y	W	$\underline{Y}$	Y	W	$\underline{Y}$
4	RX	$X_{[sy]}$ + Bb	AS	A	'not used'	–	–	RX	Ys + Bb
5	LX	$X\underline{Y}_L$	CPL	$\underline{Y}_L \rightarrow Y_L$	LX	$X\underline{Y}_L$	Y_L	LX	$X\underline{Y}_L$
6	UX	$X\underline{Y}_U$	CPU	$\underline{Y}_L \rightarrow Y_U$	UX	$X\underline{Y}_U$	Y_U	UX	$X\underline{Y}_U$
7	AR	A	CPW	$\underline{Y} \rightarrow Y$	'not used'	–	–	AR	(A)

$\underline{Y}$ = (Ys + Bb)
Ys = Selected SR (4-0) or P (17-13) concatenated with y (12-0)
sy = s (14-13) concatenated with y (12-0)
W = Whole word

L = Lower half
U = Upper half
X = Sign extension
CP = Complement
MN = Mnemonic

NORMAL b DESIGNATOR

b	MNEMONIC	DESCRIPTION
0	'blank'	No Mod
1	B1	B1
2	B2	B2
3	B3	B3
4	B4	B4
5	B5	B5
6	B6	B6
7	B7	B7

NORMAL j DESIGNATOR

j	MNEMONIC	DESCRIPTION
0	'blank'	No Skip
1	SK	Skip
2	QP	Skip if Q Positive.
3	QN	Skip if Q Negative
4	AZ	Skip if A + Zero
5	ANZ	Skip if A Not + Zero
6	AP	Skip if A Positive
7	AN	Skip if A Negative

SPECIAL $\hat{1}$ DESIGNATOR

$\hat{1}$	MN.	C f04	MN.	M f22	D f23	MN.	LLP RLP f40 f44	MN.	AQ ANQ f26 f27
0	'blank'	No Skip	'blank'	No Skip	No Skip	'blank'	No Skip	'blank'	No Skip
1	SK:	Skip	SK:	Skip	Skip	SK:	Skip	SK:	Skip
2	YLEQ:	$\underline{Y} \neq (Q)$	NOVF:	$Q_{29} = A_{29}$	No Over flow	EVEN:	Even Parity	AP:	A Positive
3	YGTQ:	$\underline{Y} > (Q)$	OVF:	$Q_{29} \neq A_{29}$	Over flow	ODD:	Odd Parity	AN:	A Negative
4	YIN:	$(A) < \underline{Y} \leq (Q)$	AZ:	$A = \pm$ Zero	$A = \pm$ Zero	AZ:	A + Zero	QZ:	Q + Zero
5	YOUT:	$\underline{Y} > (Q)$ or $\underline{Y} \leq (A)$	ANZ:	$A \neq \pm$ Zero	$A \neq \pm$ Zero	ANZ:	A Not + Zero	QNZ:	Q Not + Zero
6	YLEA:	$\underline{Y} \leq (A)$	6:	Skip	Skip	AP:	A Positive	QP:	Q Positive
7	YGTA:	$\underline{Y} > (A)$	7:	No Skip	No Skip	AN:	A Negative	QN:	Q Negative

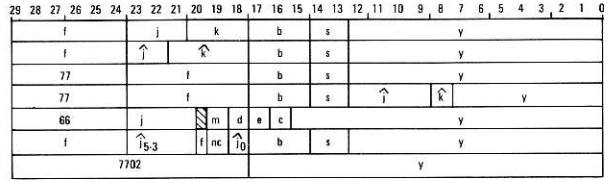
SPECIAL d,e,c,m, DESIGNATOR

DES	MNEMONIC	DESCRIPTION
d	ND	Normal Device Interrupts
e	EIS	External Interrupt & Status Word Storage
c	CI	Channel Interrupts (Class V)
m	M	Metronome, only applicable to modified processor
See Function Code 66		

ADDRESS EXTENSION (s) DESIGNATOR

s	MNEMONIC	DESCRIPTION
0	S0	SR0
1	S1	SR1
2	S2	SR2
3	S3 or 'blank'	Bit 17-13 of P

INSTRUCTION WORD FORMATS



SPECIAL PUSH, PULL $\hat{j}$ DESIGNATORS

$\hat{j}_{5-3}$	$\hat{j}_0 = 0$	$\hat{j}_0 = 1$
0	RTC	S0 : SR0
1	B1	S1 : SR1
2	B2	S2 : SR2
3	B3	AR : A Reg.

$\hat{j}_{5-3}$	$\hat{j}_0 = 0$	$\hat{j}_0 = 1$
4	B4	QR : Q Reg.
5	B5	SR : Status Reg.
6	B6	UNDEFINED
7	B7	UNDEFINED

STATUS REGISTER BIT ASSIGNMENT

IOP STATUS REGISTER	
BIT	DESCRIPTION
2-0	Device Number
3	Class 5 Interrupt Lockout
4	Class 4 Interrupt Lockout
5	Class 3 Interrupt Lockout
6	Relative Address Enable (IOPB only)
9	Scatter Interrupt Lockout (IOPB only)
10	Arithmetic Overflow
11	Interrupt Steering Enable (IOPB only)
15-12	Channel Number
18-16	Error Type*
22-19	Memory Module Number
23	I/O Error
24	Operand Error
25	Instruction Error
26	Memory Resume Error
27	Address Parity Error
28	Data Parity Error
29	I/O Data Parity Error

* ERROR TYPE CODES TABLE

Bits 18-16	DESCRIPTION
000	Input Data Error (not parity)
001	Output Data Error
010	Write Lockout Violation (modified only)
011	External Interrupt Error (not parity)
100	Input Chain Error
101	Output Chain Error
110	Read Lockout Violation (modified only)
111	I/O Write Lockout Violation (modified only)

MEMORY LOCKOUT REGISTER (MLO)

(Console Read Only)

BIT	DESCRIPTION
29-27	Interrupt Steering Register
25-21	Level Control Register (opt)
19-16	Relative Address Register
15-8	Read Lockout Register *
7-0	Write Lockout Register *

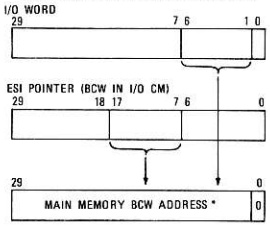
* Lockout bits represent 2048 word blocks.

I/O CONTROL MEMORY ADDRESS

BINARY	DESCRIPTION
0 0 C C C C	Input Chain Pointer
0 1 C C C C	Output Chain Pointer
1 0 C C C C	Input Buffer Control Word
1 1 C C C C	Output Buffer Control Word

NOTE: C C C C is channel number.

EXTERNAL SPECIFIED INDEXING



* Odd address is refill word

SPERRY UNIVAC DEFENSE SYSTEMS

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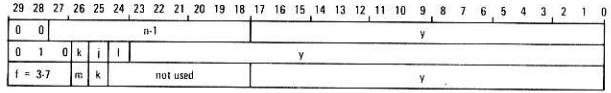
CHAIN INSTRUCTIONS

BINARY FUNCTION	SYMBOLIC CODE SEQUENCE(S)		DESCRIPTION
00	BCW	n,y	Buffer Control Word, n=number of words to be transferred
010 j=0, k=0	EFW	y,I	External Function: Whole Word, I=1 for Indirect
010 j=1, k=0	FEFW	y,I	Force External Function: Whole Word, I=1 for Indirect
010 j=0, k=1	EFH	y,I	External Function: Half Word, I=1 for Indirect
010 j=1, k=1	FEFH	y,I	Force External Function: Half Word, I=1 for Indirect
011	IOSTOP,m		I/O Stop, m=1 for Monitor Interrupt
100	IOCL	y	I/O Clear Flag: 0→ $y_{29,28}$
101	IOJ,m,k	y	I/O Jump, m=1 for Monitor Interrupt, k=1 insert channel number in y_{3-0}
110	IOSET	y	I/O Set Flag: 1→ $y_{29,28}$
111	IONOOP		I/O No Operation

CHAIN INSTRUCTION FORMATS



CONTROL MEMORY AND INTERRUPT ADDRESSES

INDIVIDUAL INTERRUPTS	ADDRESS (BINARY)			
Class V Interrupt Packet				
Status Buffer Control Word (BCW)	0	XXX	CCC	C00
Status BCW Refill	0	XXX	CCC	C10
Entrance Address	0	XXX	CCC	C11
Power On Entrance w/Auto Start Selected (IOP only)	1	00X	XX0	001
Power Tolerance Entrance (IOP only)	1	00X	XX0	010
Executive Return Entrance (IOPB only)	1	00X	XX0	011
I/O Write Lockout Entrance (IOP only)	1	00X	XX0	110
Normal Device Entrance	1	00X	XX1	001
High Priority Device Entrance (IOP only)	100001	00X	XX1	001
Monitor Clock Entrance	1	00X	XX1	010
Metronome Entrance (IOPB only)	1	00X	XX1	011
Memory Write Lockout Entrance (IOP only)	1	00X	XX1	011
Memory Read Lockout Entrance (IOP only)	1	00X	XX1	111
RTC	1	010	000	000
B_7	1	010	000	ZZZ
Monitor Clock	1	010	001	000
Used Internally	1	010	001	001
Used Internally	1	010	001	010
Push P Control Word (IOPB only)	1	010	010	000
Hardware Fault Entrance (IOP only)	1	011	000	000
Debug Mode Scatter Entrance (IOPB only)	1	011	000	000
Program Fault Entrance	1	011	000	001
Scatter Interrupt Starting Address (IOPB only)	1	011	000	010
NDRO (IOP only) through	1	010	000	000
	1	011	111	111
NDRO (IOPB only) through	1	010	100	000
	11	001	011	111
NDRO 4K (Option in IOPB only) through	1	010	100	000
	11	010	011	111

* XXX implies 3-bit device number placed in address, thus completing relative address. CCC represents channel number.

REPERTOIRE OF INSTRUCTIONS

FUNCTION CODE	NOTES*	FORMAT	SYMBOLIC CODE SEQUENCE(S)		DESCRIPTION
56		I-G	RSC,j	y,k,b,s	Replace Selective Clear: [Clear $(A)_n$ for $\underline{Y}_n = 1$] → Y & A
60 j=0		I-G	RIL		Release Interrupt Lockout
60 j=1		I-G	JRIL	y,k,b,s	Jump and Release Interrupt Lockout
60 j=2		I-G	JQP	y,k,b,s	Jump if Q Positive
60 j=3		I-G	JQN	y,k,b,s	Jump if Q Negative
60 j=4		I-G	JAZ	y,k,b,s	Jump if A + Zero
60 j=5		I-G	JANZ	y,k,b,s	Jump if A not + Zero
60 j=6		I-G	JAP	y,k,b,s	Jump if A Positive
60 j=7		I-G	JAN	y,k,b,s	Jump if A Negative
61 j=0		I-G	J	y,k,b,s	Jump
61 j=1 - 7		I-G	JC,j	y,k,b,s	Jump Conditional if Jump j is Selected
61 j=4 - 7		I-G	JSC,j	y,k,b,s	Stop Conditional if Stop j Selected and Jump on Restart
62 $\hat{j}$=0		I-OP	ICIN	$\hat{k}$,y,b,s	Load/Initiate Chain Input: $\hat{k}$ = 4 Bit Channel Number
62 $\hat{j}$=1		I-OP	ICOUT	$\hat{k}$,y,b,s	Load/Initiate Chain Output: $\hat{k}$ = 4 Bit Channel Number
62 $\hat{j}$=2		I-OP	IBIN	$\hat{k}$,y,b,s	Initiate Input or EF Buffer: $\hat{k}$ = 4 Bit Channel Number
62 $\hat{j}$=3		I-OP	IBOUT	$\hat{k}$,y,b,s	Initiate Output or EF Buffer: $\hat{k}$ = 4 Bit Channel Number
63 $\hat{j}$=0		I-OP	LCIN	$\hat{k}$,y,b,s	Load Input Chain Pointer: $\hat{k}$ = 4 Bit Channel Number
63 $\hat{j}$=1		I-OP	LCOUT	$\hat{k}$,y,b,s	Load Output Chain Pointer: $\hat{k}$ = 4 Bit Channel Number
63 $\hat{j}$=2		I-OP	LBIN	$\hat{k}$,y,b,s	Load Input BCW: $\hat{k}$ = 4 Bit Channel Number
63 $\hat{j}$=3		I-OP	LBOUT	$\hat{k}$,y,b,s	Load Output BCW: $\hat{k}$ = 4 Bit Channel Number
65 j=0		I-G	RJ	y,k,b,s	Return Jump
65 j=1 - 7		I-G	RJC,j	y,k,b,s	Return Jump Conditional if Jump j Selected
65 j=4 - 7		I-G	RJSC,j	y,k,b,s	Stop if Stop j Selected and Return Jump on Restart
66 j=0		III	STOP		Unconditional Stop
66 j=1		III	TIO	y	Terminate I/O on Channel n for $y_n = 1$
66 j=2		III	SIL,d,e,c,m	y	Disable Interrupts on Channel n for $y_n = 1$, See d,e,c,m List
66 j=3		III	RIL,d,e,c,m	y	Enable Interrupts on Channel n for $y_n = 1$, See d,e,c,m List
67 $\hat{j}$=0		I-OP	SCIN	$\hat{k}$,y,b,s	Store Chain Input Pointer: $\hat{k}$ = 4 Bit Channel Number
67 $\hat{j}$=1		I-OP	SCOUT	$\hat{k}$,y,b,s	Store Chain Output Pointer: $\hat{k}$ = 4 Bit Channel Number
67 $\hat{j}$=2		I-OP	SBIN	$\hat{k}$,y,b,s	Store Input BCW: $\hat{k}$ = 4 Bit Channel Number
67 $\hat{j}$=3		I-OP	SBOUT	$\hat{k}$,y,b,s	Store Output BCW: $\hat{k}$ = 4 Bit Channel Number
71		I-G	BSK	j,y,k,b,s	(Bj) ≠ Y, Advance Bj; (Bj) = Y, Skip NI and Clear (Bj)
72 j=0		I-G	CPFI		Clear Program Fault Indicator. On IOPB, Also Clears Hardware Fault Indicator.
72 j≠0		I-G	JBNZ	j,y,k,b,s	(Bj) ≠ 0, (Bj) − 1 → Bj and Jump to Y; (Bj) = 0 Read NI
73 j=0		I-G	JOVF	y,k,b,s	Jump if Overflow Bit Set
73 j≠0		I-G	LBJ	j,y,k,b,s	Load Bj and Jump
74 bit 20=0	4	IV	PULLT	$\hat{j}$,y,b,s	Pull Top: If Table Not Empty, Pull Top and Skip NI; else do NI
74 bit 20=1	4,2	IV	PULTB	$\hat{j}$,y,b,s	Pull Top Biased: If Table Not Empty, Pull Top and Skip NI Bias Y (Bits 6-4) by Processor Number; else do NI
75 bit 20=0	4	IV	PULLB,nc	$\hat{j}$,y,b,s	Pull Bottom: If Table Not Empty, Pull Bottom and Skip NI; else do NI
75 bit 20=1	4,2	IV	PULBB,nc	$\hat{j}$,y,b,s	Pull Bottom Biased: If Table Not Empty, Pull Bottom and Skip NI Bias Y (Bits 6-4) by Processor Number; else do NI
76 bit 20=0	4	IV	PUSHT,nc	$\hat{j}$,y,b,s	Push Top: If Table Not Full, Push Top and Skip NI; else do NI
76 bit 20=1	4,2	IV	PSHTB,nc	$\hat{j}$,y,b,s	Push Top Biased: If Table Not Full, Push Top and Skip NI Bias Y (Bits 6-4) by Processor Number; else do NI
7700	2	II-G	XM		Enable Executive Mode: Perform Executive Return
7702	2	V	PPL	y	Push P to List: P → Address Specified by (1220) (1220) + 1 → 1220, Jump to y
7703 bit 15=0	2	II-G	PLP		Pull List to P: (1220) − 1 → 1220; Jump to (1220) f
7703 bit 15=1	2	II-G	PLPR		Pull List to P and Release Interrupt Lockout: (1220) − 1 → 1220; Jump to (1220) f
7704	2	II-G	ERAJ	y,b,s	Enable Relative Addressing & Jump: 1 → Status $Register_6$; Jump to Y
7705		II-G	XR	y,b,s	Execute Remote: Execute Instruction Located at Address Y
7712	2	II-G	LAB	y,b,s	Load A Biased: (Y + Processor Number) → A
7716	2	II-G	SAB	y,b,s	Store A Biased: (A) → Y + Processor Number
7726		II-G	LMC	y,b,s	Load and Enable Monitor Clock: Y → Monitor Clock
7727		II-G	TSF	y,b,s	Test and Set Flag: If $\underline{Y}_{29,28}$ = 0, Skip NI & Set $\underline{Y}_{29,28}$: If $\underline{Y}_{29,28} \neq 0$, Do NI
7734	2	II-G	ER	y,b,s	Establish Read: (Y) → A, If $(A)_{14-0} = 0$, 1 → Bit Position Corresponding to the Processor Number Within Y_{22-15} and Skip NI. If $(A)_{14-0} \neq 0$, Execute NI
7735	2	II-G	EW	y,b,s	Establish Write: (Y) → A. If (A) = 0, 1 → Bit Position Corresponding to the Processor Number Within Y_{7-0} and Skip NI. If (A) ≠ 0, Execute NI.
7736	2	II-G	RR	y,b,s	Relinquish Read; 0 → Bit Position Corresponding to the Processor Number Within Y_{22-15}
7737	2	II-G	RW	y,b,s	Relinquish Write; 0 → Bit Position Corresponding to the Processor Number Within Y_{7-0}
7742 $\hat{k}$=1		II-OP	LST	y,b,s	Load Status Register: (Y) → Status Reg.
7743 $\hat{k}$=1	2	II-OP	LML	$\hat{j}$,y,b,s	Load Memory Lockout Register: $(Y)_{15-0}$ → MLO $\hat{j}$
7744 $\hat{k}$=0	2	II-OP	SMLQ	$\hat{j}$	Store Memory Lockout Register in Q: (MLO $\hat{j}$) → Q_{15-0} (RAR $\hat{j}$) → Q_{19-16} 0 → Q_{29-20}
7744 $\hat{k}$=1	2	II-OP	SML	$\hat{j}$,y,b,s	Store Memory Lockout Register: (MLO $\hat{j}$) → Y_{15-0} (RAR $\hat{j}$) → Y_{19-16} 0 → Y_{29-20}
7745 $\hat{k}$=0		II-OP	SSTQ		Store Status Register: (Status Reg.) → Q
7745 $\hat{k}$=1		II-OP	SST	y,b,s	Store Status Register: (Status Reg.) → Y
7746 $\hat{k}$=0	2	II-OP	DRPIR		Disable Relative Processor Interrupt Register: 0 → $Status\ Register_{11}$
7746 $\hat{k}$=1	2	II-OP	ERPIR		Enable Relative Processor Interrupt Register: 1 → $Status\ Register_{11}$
7747 $\hat{k}$=0	2	II-OP	LRPIR	$\hat{j}$,y	Load Relative Processor Interrupt Register: Y_{2-0} → RP $\hat{j}$
7747 $\hat{k}$=1	2	II-OP	SRPIR	$\hat{j}$	Store Relative Processor Interrupt Register: (RP $\hat{j}$) → Q_{2-0}, 0 → Q_{29-3}
7750	2	II-OP	DRAD		Disable Relative Address Designator: 0 → $Status\ Register_6$
7751	2	II-OP	LRAR	$\hat{j}$,y	Load Relative Address Register Y_{3-0} → RAR $\hat{j}$
7760		II-OP	LSR	j,y,$\hat{k}$,b,s	Load Address Extension Register SR $\hat{j}$ ($\hat{j}$ = 0,1,2): $\hat{k}$ = 0: Y_{4-0} → SR $\hat{j}$ $\hat{k}$ = 1: $(Y)_{4-0}$ → SR $\hat{j}$
7770		II-OP	SSR	$\hat{j}$,y,$\hat{k}$,b,s	Store Address Extension Register SR $\hat{j}$ ($\hat{j}$ = 0,1,2): $\hat{k}$ = 0: (SR $\hat{j}$) → Q_{4-0} and Clear Q_{29-5} $\hat{k}$ = 1: (SR $\hat{j}$) → Y_{4-0} and Clear Y_{14-5}

NOTES

1 See List of Special $\hat{j}$ Designators
2 Instruction may be used on IOPB only
3 Instruction may be used on IOP only
4 See List of Special Push, Pull $\hat{j}$ Designators. nc = Non-Circular (Opt.) Otherwise Circular. If bit 20 = 1, Y_{6-4} must be 111
5 Instruction may be used only on IOPB with 4K NDRO option

FUNCTION CODE	NOTES*	FORMAT	SYMBOLIC CODE SEQUENCE(S)		DESCRIPTION
01		I-G	SRQ,j	y,k,b,s	Shift Right (Q) by Y
02		I-G	SRA,j	y,k,b,s	Shift Right (A) by Y
03		I-G	DSR,j	y,k,b,s	Double Shift Right (AQ) by Y
04	1	I-G	C $\hat{j}$	y,k,b,s	Compare Y with A, Q or A & Q
05		I-G	SLQ,j	y,k,b,s	Shift Left (Q) by Y
06		I-G	SLA,j	y,k,b,s	Shift Left (A) by Y
07		I-G	DSL,j	y,k,b,s	Double Shift Left (AQ) by Y
10		I-G	LQ,j	y,k,b,s	Load Q: Y → Q
10 y=k=0		I-G	ZQ,j		Clear Q: 0 → Q
11		I-G	LA,j	y,k,b,s	Load A: Y → A
11 y=k=0		I-G	ZA,j		Clear A: 0 → A
12		I-G	LB	j,y,k,b,s	Load Bj: Y → Bj
12 y=k=0		I-G	ZB	j	Clear Bj: 0 → Bj
12 j=0		I-G	NOOP		No Operation
13		I-G	ENY	j,y,k,b,s	Encode Y: Y (encoded) → Bj
14 k≠0		I-G	SQ,j	y,k,b,s	Store Q: (Q) → Y
14 k=0		I-G	CPQ, j		Complement Q: (Q)' → Q
15 k≠4		I-G	SA, j	y,k,b,s	Store A: (A) → Y
15 k=4		I-G	CPA,j		Complement A: (A)' → A
16		I-G	SB	j,y,k,b,s	Store Bj: (Bj) → Y
16 j=0		I-G	SZ	y,k,b,s	Store Zero: 0 → Y
17 k=0		I-G	STIME	j	Select Timing Source: j = Device Number
17 k=1		I-G	NINT	j,y,b,s	Normal Priority Interrupt: j = Device Number: If Y 29,28 = 0 (A) → Y, INTERRUPT j and SKIP NI: If Y 29,28 ≠ 0, DO NI
17 k=2	3	I-G	HINT	j,y,b,s	High Priority Interrupt: j = Device Number: If Y 29,28 = 0 (A) → Y, INTERRUPT j and SKIP NI: If Y 29,28 ≠ 0, DO NI
17 k=2	5	I-G	LLC	y	Load Level Control Register y_{4-0} → Level Control Register
17 k=4	2	I-G	NDROD		NDRO Disable: Clear NDRO Enable F/F
17 k=5	2	I-G	NDROE		NDRO Enable: Set NDRO Enable F/F
17 k=6	2	I-G	IPSS	j	Interprocessor Stop: Signal → Processor j
17 k=7	2	I-G	SCATI		Scatter Interrupt: Cause Interrupt to all Processors
20		I-G	AA,j	y,k,b,s	Add to A: (A) + Y → A
21		I-G	ANA,j	y,k,b,s	Add Negative to A: (A) − Y → A
22 k≠7	1	I-G	M $\hat{j}$	y,k,b,s	Multiply: (Q) · Y → AQ
23 k≠7	1	I-G	D $\hat{j}$	y,k,b,s	Divide: (AQ) ÷ Y → Q: Remainder → A
24		I-G	RA,j	y,k,b,s	Replace Add: (A) + Y → Y & A
25		I-G	RAN,j	y,k,b,s	Replace Add Negative to A: (A) − Y → Y & A
26	1	I-G	AQ $\hat{j}$	y,k,b,s	Add to Q: (Q) + Y → Q
27	1	I-G	ANQ $\hat{j}$	y,k,b,s	Add Negative to Q: (Q) − Y → Q
30		I-G	LSUM,j	y,k,b,s	Load Sum: Y + (Q) → A
31		I-G	LDIF,j	y,k,b,s	Load Difference: Y − (Q) → A
34		I-G	RSUM,j	y,k,b,s	Replace Sum: Y + (Q) → Y & A
35		I-G	RDIF,j	y,k,b,s	Replace Difference: Y − (Q) → Y & A
36		I-G	RI,j	y,k,b,s	Replace Increment: Y + 1 → Y & A
37		I-G	RD,j	y,k,b,s	Replace Decrement: Y − 1 → Y & A
40	1	I-G	LLP $\hat{j}$	y,k,b,s	Load Logical Product: L [Y(Q)] → A
43		I-G	CM,j	y,k,b,s	Compare Mask: (A) − L [Y(Q)] → A Sense j, (A) + L [Y (Q)] → A
44	1	I-G	RLP $\hat{j}$	y,k,b,s	Replace Logical Product: L [Y(Q)] → Y & A
50		I-G	OR,j	y,k,b,s	Inclusive OR: Set $(A)_n$ for $\underline{Y}_n = 1$
51		I-G	XOR,j	y,k,b,s	Exclusive OR: Complement $(A)_n$ for $\underline{Y}_n = 1$
52 k≠7		I-G	SC,j	y,k,b,s	Selective Clear: Clear $(A)_n$ for $\underline{Y}_n = 1$
54		I-G	ROR,j	y,k,b,s	Replace OR: [Set $(A)_n$ for $\underline{Y}_n = 1$] → Y & A
55		I-G	RXOR,j	y,k,b,s	Replace Exclusive OR: [CPL $(A)_n$ for $\underline{Y}_n = 1$] → Y & A

FUNCTION CODE	NOTES*	FORMAT	SYMBOLIC CODE SEQUENCE(S)		DESCRIPTION
7726		II-G	LMC	y,b,s	Load and Enable Monitor Clock: Y → Monitor Clock
7727		II-G	TSF	y,b,s	Test and Set Flag: If $\underline{Y}_{29,28}$ = 0, Skip NI & Set $\underline{Y}_{29,28}$: If $\underline{Y}_{29,28} \neq 0$, Do NI
7734	2	II-G	ER	y,b,s	Establish Read: (Y) → A, If $(A)_{14-0} = 0$, 1 → Bit Position Corresponding to the Processor Number Within Y_{22-15} and Skip NI. If $(A)_{14-0} \neq 0$, Execute NI
7735	2	II-G	EW	y,b,s	Establish Write: (Y) → A. If (A) = 0, 1 → Bit Position Corresponding to the Processor Number Within Y_{7-0} and Skip NI. If (A) ≠ 0, Execute NI.
7736	2	II-G	RR	y,b,s	Relinquish Read; 0 → Bit Position Corresponding to the Processor Number Within Y_{22-15}
7737	2	II-G	RW	y,b,s	Relinquish Write; 0 → Bit Position Corresponding to the Processor Number Within Y_{7-0}
7742 $\hat{k}$=1		II-OP	LST	y,b,s	Load Status Register: (Y) → Status Reg.
7743 $\hat{k}$=1	2	II-OP	LML	$\hat{j}$,y,b,s	Load Memory Lockout Register: $(Y)_{15-0}$ → MLO $\hat{j}$
7744 $\hat{k}$=0	2	II-OP	SMLQ	$\hat{j}$	Store Memory Lockout Register in Q: (MLO $\hat{j}$) → Q_{15-0} (RAR $\hat{j}$) → Q_{19-16} 0 → Q_{29-20}
7744 $\hat{k}$=1	2	II-OP	SML	$\hat{j}$,y,b,s	Store Memory Lockout Register: (MLO $\hat{j}$) → Y_{15-0} (RAR $\hat{j}$) → Y_{19-16} 0 → Y_{29-20}
7745 $\hat{k}$=0		II-OP	SSTQ		Store Status Register: (Status Reg.) → Q
7745 $\hat{k}$=1		II-OP	SST	y,b,s	Store Status Register: (Status Reg.) → Y
7746 $\hat{k}$=0	2	II-OP	DRPIR		Disable Relative Processor Interrupt Register: 0 → $Status\ Register_{11}$
7746 $\hat{k}$=1	2	II-OP	ERPIR		Enable Relative Processor Interrupt Register: 1 → $Status\ Register_{11}$
7747 $\hat{k}$=0	2	II-OP	LRPIR	$\hat{j}$,y	Load Relative Processor Interrupt Register: Y_{2-0} → RP $\hat{j}$
7747 $\hat{k}$=1	2	II-OP	SRPIR	$\hat{j}$	Store Relative Processor Interrupt Register: (RP $\hat{j}$) → Q_{2-0}, 0 → Q_{29-3}
7750	2	II-OP	DRAD		Disable Relative Address Designator: 0 → $Status\ Register_6$
7751	2	II-OP	LRAR	$\hat{j}$,y	Load Relative Address Register Y_{3-0} → RAR $\hat{j}$
7760		II-OP	LSR	j,y,$\hat{k}$,b,s	Load Address Extension Register SR $\hat{j}$ ($\hat{j}$ = 0,1,2): $\hat{k}$ = 0: Y_{4-0} → SR $\hat{j}$ $\hat{k}$ = 1: $(Y)_{4-0}$ → SR $\hat{j}$
7770		II-OP	SSR	$\hat{j}$,y,$\hat{k}$,b,s	Store Address Extension Register SR $\hat{j}$ ($\hat{j}$ = 0,1,2): $\hat{k}$ = 0: (SR $\hat{j}$) → Q_{4-0} and Clear Q_{29-5} $\hat{k}$ = 1: (SR $\hat{j}$) → Y_{4-0} and Clear Y_{14-5}

NOTES

$\underline{Y}$ = The Operand Regardless of Source, i.e., y, (Y), Y or sy
Y = The Source or Destination of the Operand, i.e., y extended plus Bb

INTERRUPT STATUS WORD FORMAT

Bits 27	26	25	
0	0	0	External Interrupt Parity Error Interrupt
0	0	1	Input Buffer Parity Error Interrupt
0	1	0	Input Chain Monitor Interrupt
0	1	1	Output Chain Monitor Interrupt
1	0	0	External Interrupt
1	0	1	Not Used
1	1	0	Not Used
1	1	1	Not Used

PUSH, PULL CONTROL PARAMETER WORDS

	29 28 27 26 25 24 23 22 21 20 19 18	17 16 15 14 13 12 11 10 9 8 7 6	5 4 3 2 1 0
Y*	TOP SPACE COUNT (TSC)	TOP ADDRESS POINTER (TAP)	
Y + 1	BOTTOM SPACE COUNT (BSC)	BOTTOM ADDRESS POINTER (BAP)	
Y + 2	LIST LENGTH (LL)	BASE ADDRESS (BA)	

*Y must be divisible by four