

UNIVAC 1824 COMPUTER INSTRUCTION REPERTOIRE

	F	B	X	SYMBOLIC	FUNCTION	TIME μ sec.
ENTER	12	B	0	ENT.B ⁿ .Y	(Y) \rightarrow B ⁿ	12
	12	B	1	ENT.B ⁿ .Y	Y \rightarrow B ⁿ	8
	13	S	X	ENT.SP ⁿ .Y	(Y) \rightarrow SP ⁿ	12
	25	B	X	ENT.A.Y	(Y) \rightarrow A	8
	27	B	X	ENT.Q.Y	(Y) \rightarrow Q	8
	35	B	0	ENT.X.Y	(Y) ₁₅₋₂₂ \rightarrow X Register	8
	35	B	1	ENT.X.Y	Y \rightarrow X Register	4
STORE	10	3	X	CLR.Y	Zeros \rightarrow Y	12
	24	B	X	STR.A.Y	(A) \rightarrow Y	8
	26	B	X	STR.Q.Y	(Q) \rightarrow Y	8
	34	B	X	STR.X.Y	(X) \rightarrow Y	8
ARITHMETIC	11	0	X	DEC.Y	(Y) - 1 \rightarrow Y	12
	11	0	X	INC.Y	(Y) + 1 \rightarrow Y	12
	11	2	X	RAD.Y	(Y) \div (A) \rightarrow Y	12
	20	B	X	ADD.AQ.Y*	(AQ) \div ((Y-1), (Y)) \rightarrow AQ	12
	21	B	X	ADD.A.Y	(A) + (Y) \rightarrow A	8
	22	B	X	SUB.AQ.Y*	(AQ) - ((Y-1), (Y)) \rightarrow AQ	12
	23	B	X	SUB.A.Y	(A) - (Y) \rightarrow A	8
	30	1	1	SQR.D ⁿ **	$\sqrt{(A)} \rightarrow Q, R \rightarrow A$	192
	36	B	X	MPY.Y	(A)(Y) \rightarrow AQ	44-92
37	B	X	DIV.Y	(AQ) \div (Y) \rightarrow Q, R \rightarrow A	128	
MISC.	30	0	0	LGP.D ⁿ **	L(A Q) \rightarrow A	8
	30	1	0	STP.N	Stop if switch N is set	8

NOTES:

*Y must specify an even address.

**0 indicates no operand required.

A—a 24-bit accumulator register.

B—indicates B bits may be used to select index register modification. B=1, 2, or 3 for mod. B=0 for no mod. To use the modification, add .Bⁿ to symbolic code and 4 μ s to time.

C—indicates B and X bits used to designate I/O channel.

B=2, X=0 -C=5; B=1, X=0 -C=6; B=0, X=1 -C=7.

P—indicates B or X bits used as part of operand Y.

Q—a 24-bit quotient register.

	F	B	X	SYMBOLIC	FUNCTION	TIME μ sec.	
SKIP	Non-Modifying	04	B	X	NSK.Y	Skip if (Y) = 0	8
		06	B	X	ZSK.Y	Skip if (Y) = 0	8
		10	0	X	DEC.Y.SK	(Y) - 1 \rightarrow Y, Skip if (Y) < 0	12-16
		10	1	X	INC.Y.SK	(Y) + 1 \rightarrow Y, Skip if (Y) < 0	12-16
		10	2	X	RAD.Y.SK	(Y) \div (A) \rightarrow Y, Skip if (Y) < 0	12-16
JUMP	Uncond.	00	B	P	GJP.Y	Y \rightarrow P ₇₋₁₅	4
		01	B	X	IJP.Y	(Y) ₁₅₋₂₂ \rightarrow P ₃₋₁₅	8
		02	P	P	DJP.Y	Y \rightarrow P ₃₋₁₅	4
		03	B	X	RJP.Y	P + 1 \rightarrow 10, (Y) ₁₅₋₂₂ \rightarrow P ₇₋₁₅	12
	Cond.	05	B	P	NJP.Y	If (A) < 0, Y \rightarrow P ₇₋₁₅	4
07		B	P	ZJP.Y	If (A) = 0, Y \rightarrow P ₇₋₁₅	8	
SHIFT	I/O	30	0	1	XCH.D ⁿ **	(A) \rightarrow Q, (Q) \rightarrow A	12
		31	B	X	SCF.Y	Scale (AQ), (K) \rightarrow Y ₁₅₋₂₃	12-52
		32	B	0	RSR.Y	Shift (AQ) right by (Y) ₁₅₋₂₃	12-52
		32	0	1	RSH.Y	Shift (AQ) right by Y	8-48
		33	B	0	LSH.Y	Shift (AQ) left by (Y) ₁₅₋₂₃	12-52
		33	0	1	LSH.Y	Shift (AQ) left by Y	8-48
I/O	11	3	X	UIO.Y	Update Incr. Register Y	12	
	14	C	C	OUT.C ⁿ .Y	(Y) \rightarrow Output Channel C	8	
	15	C	C	INP.C ⁿ .Y	Input Channel C \rightarrow Y	8	
	16	B	X	OUT.Y	Output according to (Y)	12	
	17	B	X	INP.Y	Input according to (Y)	12	

S—indicates B bits used to select special register 0, 1, 2, or 3.

X—indicates X bit used for extension register modification. X=1 use mod. X=0 no mod.

AQ—a 48-bit double precision accumulator.

UNIVAC 1824 COMPUTER

INSTRUCTION WORD FORMAT

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
F					B		X	Y							

INDIRECT INPUT/OUTPUT WORD FORMAT

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
Channel Selection											Not Used		X	Data Address									

SPECIAL ADDRESS ASSIGNMENTS

00000	B Box No. 0 (non-modifying)
00001	B Box No. 1
00002	B Box No. 2
00003	B Box No. 3
00004	Special Register No. 0
00005	Special Register No. 1
00006	Special Register No. 2
00007	Special Register No. 3
00010	P Storage for Return Jump
00016	P Storage for Real Time Interrupt
00017	P Storage for External Interrupt
04376	Real Time Interrupt Entrance Address
04377	External Interrupt Entrance Address
47777	Master Reset Address

TYPE C INCREMENTAL INPUTS

N*+3 Ψ _g	N*+12 _g Δ VX
N*+4 Θ _g	N*+13 _g Δ VY
N*+5 \emptyset _g	N*+14 _g Δ VZ

TYPE C I/O CHANNEL ASSIGNMENTS

CHANNEL	FUNCTION	BITS
DI 6	Input Discretes 24-34, 41-47	18
DI 7	Input Discretes 0-23	24
II 9	Serial Register	24
II 10	Input Holding Register	19
DO 5	Serial Data (32KC)	24
DO 6	Output Discretes 24-43	20
DO 7	Output Discretes 0-23	24
IO 0	Release External Interrupt Lockout	0
IO 1	Initiate Serial Register Shift	0
IO 2	Telemetry Data (128 KC)	24
IO 3	Output Discretes 44-47 (44 Resets to 0)	4
IO 4	Output Holding Register (Channel 1)	14
IO 5	Output Holding Register (Channel 2)	14
IO 6	Output Holding Register (Channel 3)	14
IO 7	D/A Converter (Channel 2)	7
IO 8	D/A Converter (Channel 1)	7
IO 9	D/A Converter (Channel 4)	7
IO 10	D/A Converter (Channel 3)	7
IO 11	D/A Converter (Channel 5)	7

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*N can be any address modulo 20_g from 00020_g through 00760_g.