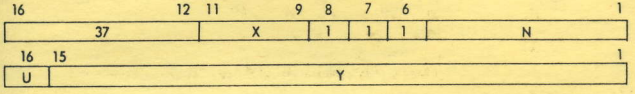
Internal Test (X = 0,1,3; C = 1; K = 0) - Test for any or all of conditions specified by "1's" in XIO Output Data Word. Skip if all conditions tested are zero.

Internal Set (X = 0,1,3; C = 1; K = 1) - Set or clear flipflops specified by "1's" in XIO Output Data Word.

Output Data Word Bit	Used In Set or Test	Function
1	Set	Set ("1")/Clear ("0")
2–4	–	Unused
5	Test	Sense Switch 1
6	Test	Sense Switch 2
7	Test	Sense Switch 3
8	Test	Sense Switch 4
9	Test	Overflow flip-flop (cleared when tested)
10	Set and Test	Scanned and Programmed I/O Interrupt Allow flip-flop
11	Set and Test	External Priority Interrupt Allow flip-flop
12–16	–	Unused

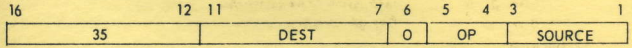
MISCELLANEOUS INSTRUCTIONS

OCTAL	MNE	FORMAT	DESCRIPTION
34–37	PIn	L	Programmed Instruction



First Word	Bits 16-12	All ones to specify long format
	Bits 11- 9	Address modification
	Bits 8- 6	Specify a PIn instruction
	Bits 5- 1	N is used to form the PI address, N + 40_8 = Address
Second Word	Bit 16	Not used
	Bits 15- 1	Base operand address

35 MOV S Move



Source	Code	Register	Destination	Code	Register
0	Z	Zeros	Bit 11 = 1	4	X4
1	1	X1	Bit 10 = 1	2	X2
2	2	X2	Bit 9 = 1	1	X1
3	4	X4	Bit 8 = 1	A	A
4,6	A	A	Bit 7 = 1	E	E
5,7	E	E			

35	MOV	S	Move Source to Destination OP = 00
35	CMP	S	Complement Source And Move OP = 01
35	MAO	S	Add One to Source And Move OP = 10
35	NEG	S	Negate Source And Move OP = 11

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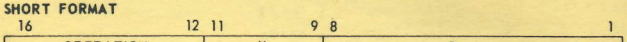
INSTRUCTION FORMAT

SHORT FORMAT

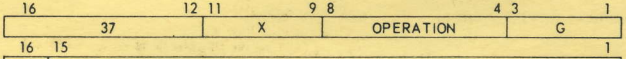


Bits 16-12	Instruction to be performed (37 8 specifies long format)
Bits 11- 9	Address modification
Bits 8- 1	Operand or relative operand address

Modifier Bits

X	Address	
0	m = P + D	(D is two's complement)
1	m = X1 + D	
2	m = X2 + D	
3	m = X1 + X2 + D	
4	m = Indirect via P + D	
5	m = Indirect via X1 + D	
6	m = X4 + D	
7	Use D as the operand (D is 8 bits of positive magnitude)	

LONG FORMAT



First Word

Bits 16-12	All ones to specify LONG format
Bits 11- 9	Address modification
Bits 8- 4	Instruction to be performed
Bits 3- 1	Designator bits

Second Word

Bit 16	Sign of a 15-bit two's complement number when X = 7. Ignored when X = 0 – 6.
Bits 15- 1	Base operand address when X = 0 – 6.

Modifier Bits

X	Address
0	m = Y
1	m = X1 + Y
2	m = X2 + Y
3	m = X1 + X2 + Y
4	m = Indirect via Y
5	m = Indirect via X1 + Y
6	m = X4 + Y
7	m = P + 1 Use full 16 bits as a signed operand

REPERTOIRE

LOAD AND STORE INSTRUCTIONS

OCTAL	MNE	FORMAT		DESCRIPTION
10	LDA	S/L	Load A	G = 4,6	(m) → A
11	LDE	S/L	Load E	G = 5,7	(m) → E
10, 11	LDXn	L	Load Index "n"	G = 1,2,3	(m) → Xn
14	DLD	S/L	Double Load AE	G = 0	(m) → A, (m + 1) → E
14	CLS	L	Clear Protect Single	G = 4	(m) → A, (m + 1) → E, change protect status
14	CLD	L	Clear Protect Double	G = 6	
14	PRS	L	Protect Single	G = 5	
14	PRD	L	Protect Double	G = 7	
22	STA	S/L	Store A	G = 4,6	(A) → m
23	STE	S/L	Store E	G = 5,7	(E) → m
20	DST	S/L	Double Store AE		(A) → m, (E) → m + 1
22,23	STXn	L	Store Index "n"	G = 1,2,3	(Xn) → m
22,23	STZ	L	Store Zero	G = 0	"0's" → m

ARITHMETIC INSTRUCTIONS

15	ADD	S/L	Add		(A) + (m) → A
24	SUB	S/L	Subtract		(A) − (m) → A
16	MPY	S/L	Multiply		(A) • (m) → AE
21	DAD	S/L	Double Add		(AE) + (m, m + 1) → AE
30	DVD	S/L	Divide		(AE) ÷ (m) → E (Quot.) A (Rem.); skip if not overflow divide
33	AXDn	S	Augment Index "n" and Test	X = 1,2,6	(Xn) + D → Xn, skip if result > (P + 1)

LOGICAL INSTRUCTIONS

12	LOR	S/L	Logical OR	(E) ⊕ (m) → A
13	AND	S/L	Logical AND	(E) ⊙ (m) → A
31	XOR	S/L	Exclusive OR	[(E) ⊙ ($\overline{m}$)] ⊕ [($\overline{E}$) ⊙ (m)] → A

JUMP, BRANCH, SKIP INSTRUCTIONS

00	JMP	S/L	Jump		m → P
01	JCI	S/L	Jump and Clear Interrupt		m → P, Clear Interrupt
07	JLZ	S/L	Jump if (A) < 0		m → P, if (A) < 0
06	JEZ	S/L	Jump if (A) = 0		m → P, if (A) = 0
05	JGZ	S/L	Jump if (A) > 0		m → P, if (A) > 0
03	XEC	S/L	Execute	G = 0, 2–7	Execute a remote instruction.
25	KAL	S/L	Skip "A" Low		If (A) < (m), skip
26	KAQ	S/L	Skip "A" Equal		If (A) = (m), skip
27	KAH	S/L	Skip "A" High		If (A) > (m), skip
17	IMT	S/L	Increment Memory and Test	G = 1	(m) + 1 → m, skip if result = 0 or changes sign
17	AMTn	L	Add to Memory and Test	G = 0, 2–7	(m) + G → m, skip if result = 0 or changes sign
04	JTB	S/L	Jump and Test Bits		(m + k) → P, k = shift count generated
02	RTJ	S/L	Return Jump		short: P + 1 → m, m + 1 → P long: P + 2 → m, m + 1 → P

MONITOR ENTRY INSTRUCTION

OCTAL	MNE	FORMAT		DESCRIPTION
03	SMM	L	Set Monitor Master	X = 4, G = 1 Execute (Indirect) instruction specified in loc. 00001.

SHIFT INSTRUCTIONS

34	RSA	S	Arithmetic Right Shift A	X = 0, D8 = 0 or 1
34	RSD	S	Arithmetic Right Shift AE	X = 2, D8 = 0 or 1
34	LSA	S	Arithmetic Left Shift A	X = 4, D8 = 0
34	LSD	S	Arithmetic Left Shift AE	X = 6, D8 = 0
34	RLA	S	Logical Right Shift A	X = 1, D8 = 0
34	RLD	S	Logical Right Shift AE	X = 3, D8 = 0 or 1
34	LLA	S	Logical Left Shift A	X = 5, D8 = 0
34	LLD	S	Logical Left Shift AE	X = 7, D8 = 0
34	CSA	S	Circular Left Shift A	X = 5, D8 = 1
34	CSD	S	Circular Left Shift AE	X = 7, D8 = 1
34	TRN	S	Transpose	X = 1, D8 = 1
34	NRM	S	Normalize AE	X = 6, D8 = 1
34	TAL	S	Tally	X = 4, D8 = 1
34	NOP	S	No Operation	D1-7 = 0, shift count of zero

STATUS INSTRUCTIONS

33	SST	S	Store Status	X = 7, D1 = 0
33	LST	S	Load Status	X = 7, D1 = 1

INPUT/OUTPUT INSTRUCTION

36	XIO	S	External Input/Output
16		12	11 9 8 7 6 1

36	X	C	K	ED ADDRESS

Bits 11–9

X	Function
0	Contents of P + 1 to I/O Lines
1	Contents of Address in P + 1 to I/O Lines
2	0's to I/O Lines 2-16, D8 to I/O Line 1
3	Contents of A Register to I/O Lines
4	I/O Lines to P + 1
5	I/O Lines to Address in P + 1
6	Direct XIO - Stop Bit in Control Word
7	Compatible XIO - Send COMPLETE to ED I/O Lines to A Register

Bit 8

C	Function
0	Compatible XIO (Unless X = 2)
1	Direct XIO

Bit 7

K	Function
0	Direct XIO - Skip if ED Ready
1	No Skip - Operation occurs regardless of Busy (C = 1, K = 1 to specify Status Word input for Direct XIO. Any direct input is Status Word input in Compatible XIO.)

Bits 6–1 ED Address - Address of external device (01_8–77_8) to which the instruction is directed.

ED Address 00_8 is used for internal XIO. The three internal functions are:

Internal Input (X = 4,5,7; C = 1; K = 1) - Input contents of interrupt scanner in bits 6–1 of Input Word. (Bit 11 of Input Word = 1, bits 7–10 & 12–16 = 0.)