## AN/UYK-7(V) Diagnostic
### Supplementary Tests

<table>
<thead>
<tr>
<th>A0</th>
<th>IOC No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>Normal Output</td>
</tr>
<tr>
<td>A2</td>
<td>Bus Test Selected Memory Banks</td>
</tr>
<tr>
<td>A3</td>
<td>0 Bus Test Selected Memory Banks</td>
</tr>
<tr>
<td>A4</td>
<td>Channels-To-Test</td>
</tr>
<tr>
<td>A5</td>
<td>ESA Channel-To-Test</td>
</tr>
<tr>
<td>A6</td>
<td>Banks-To-Test</td>
</tr>
<tr>
<td>A7</td>
<td>Subtest Select</td>
</tr>
<tr>
<td>S1</td>
<td>Load Bias</td>
</tr>
<tr>
<td>P</td>
<td>0200 + S1</td>
</tr>
</tbody>
</table>

### A7 Bit

<table>
<thead>
<tr>
<th>A7 Bit</th>
<th>Subtest Selected</th>
<th>Selectable Registers</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>See Para. 4.23.3.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>See Para. 4.23.3.3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>See Para. 4.23.3.4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>See Para. 4.23.3.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>See Para. 4.23.3.6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>See Para. 4.23.3.7</td>
</tr>
</tbody>
</table>

### Options

<table>
<thead>
<tr>
<th>Jump 1</th>
<th>Jump 2</th>
<th>Jump 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stop 4</td>
<td>Stop 5</td>
<td>Stop 6</td>
</tr>
<tr>
<td>Stop 7</td>
<td>Ending address for all tests at 6 Stop is P = 400346 (S1 + 346)</td>
<td></td>
</tr>
</tbody>
</table>
ABBREVIATED OPERATING INSTRUCTIONS
FOR AN/UYK-7(V) COMPUTER DIAGNOSTICS
(REFER TO NAVSEA 0967-024-5453 PART 1, 2, 3, CHANGE 5)

Bootstrap Load
A3 = Load Channel
S1 = Load Bias
S6 = Bias + 37700

CPU Diagnostic (2 seconds)
A0 = IOC No.
S1 = Load bias
P = 0 + S1

IOC/OA Diagnostic (25 seconds)
A0 = IOC No.
A1 = Channels to Test
A2 = IC Channels to Test (Must Also Be Selected in A1)
A3 = End-Around-Channels to Test (Must Also Be Selected in A1)
S3 = 20,000 + Load Bias
P = 0 + S3

Memory Diagnostic (Core Memory 25 Seconds Per Module, DDMFM 2 minutes Per Module)
A0 = IOC No.
A6 = Banks to Test (Bits 0-15 For Core, Bits 16-31 For DDMFM)
A7 = Memory Options
  Bit 31 = Bypass 1 Bus
  Bit 30 = Bypass Pattern Tests
S2 = 30,000 + Load Bias
P = 0 + S2

Key Options
Jump 1 = Interleaved Core Memory
Jump 2 = End-Around-Channels
Jump 3 = Loop On Diagnostic
Stop 4 = Unexpected Class I Interrupt
Stop 5 = Error Stop
Stop 6 = End of Individual Diagnostic
Stop 7 = End of Individual Subtest

Ending Addresses
Separated Tests
CPU = 411303 (S1 + 11303)
IOC = 7000 (S0 + 7000)
MEM = 1000122 (S2 + 122)

Confidence Test
CPU = 411303 (S1 + 11303)
IOC = 7000 (S0 + 7000)
MEM = 2000122 (S4 + 122)

Confidence Test
A0 = IOC No.
A1 = Channels to Test
A2 = IC Channels (Must Also Be Selected in A1)
A3 = End-Around-Channels (Must Also Be Selected in A1)
A6 = Banks to Test (Bits 0-15 For Core, Bits 16-31 For DDMFM)
A7 = Memory Options
  Bit 31 = Bypass 1 Bus
  Bit 30 = Bypass Pattern Tests
S1 = Load Bias
P = S1 + 17770