

I/O CONTROLLER COMMANDS

Code	Mnemonic	NAME	DESCRIPTION	UF**	Time $\mu$ s
10	IB	Initiate Input Buffer on Cj	(Y)→CMA* 0+; Activate Input	1	3.25
11	OB	Initiate Output Buffer on Cj	(Y)→CMA* 20+; Activate Output	1	3.25
12	FB	Initiate EF Buffer on Cj	(Y)→CMA* 40+; Activate EF	1	3.25
13	XB	Initiate EI Buffer on Cj	(Y)→CMA* 60+; Activate EI	1	3.25
14 k=0	TIB	Terminate Input Buffer on Cj	Terminate Input m=0 Suppress	2	3.0
14 k=1	TOB	Terminate Output Buffer on Cj	Terminate Output Requested Interrupt;	2	3.0
14 k=2	TFB	Terminate EF Buffer on Cj	m=1 Allow	2	3.0
14 k=3	TXB	Terminate EI Buffer on Cj	Terminate EI Interrupt	2	3.0
15 k=0	IMIR	Set Input Monitor Interrupt Request on Cj	Set Input Monitor Interrupt on Chan j	3	2.5
15 k=1	OMIR	Set Output Monitor Interrupt Request on Cj	Set Output Monitor Interrupt on Chan j	3	2.5
15 k=2	FMIR	Set EF Monitor Interrupt Request on Cj	Set EF Monitor Interrupt on Chan j	3	2.5
15 k=3	XMIR	Set EI Monitor Interrupt Request on Cj	Set EI Monitor Interrupt on Chan j	3	2.5
16 k=0	ACI	Activate Input Chain on Cj	(Y)→Command Address Pointer Field	4	2.5
16 k=1	AOC	Activate Output Chain on Cj	(Y)→Data 39-50 of CMA* 20k+;	4	2.5
16 k=2	AFC	Activate EF Chain on Cj	Activate Chain	4	2.5
16 k=3	AFC	Activate EI Chain on Cj	Activate Chain	4	2.5
17 m=0	TST	Test Set Cleared	If (Y) <sub>0</sub> =0, SKIP; Else NI	7	4.0
17 m=1	TBS	Test Bit Set	If (Y) <sub>0</sub> ≠ 0, SKIP; Else NI	6	2.5
20	JIO	Jump (Input/Output)	(Y)→Command Address Pointer or CAR †	5	3.25
21	LICM	Load IOC Control Memory	(Y)→IOC Control Memory Address k	5	3.25
22	ILTC	Load Real Time Clock	(Y)→k	4	4.0
24	SICM	Store IOC Control Memory	(Y)→IOC Control Memory <sub>0</sub> →Y	5	3.25
25	IBS	Set Bit	1→Y <sub>0</sub>	5	3.25
26	IBS	Clear Bit	0→Y <sub>0</sub>	5	3.25
27	ITSF	Test and Set Flag	1→Y <sub>0</sub> ; If (Y) <sub>0</sub> was Originally Cleared, Skip; Else NI	6	3.25

†Command Address Register  
\*Control Memory Address

\*\*ULTRA Form

1—i, k, c, m    4—j, y, c  
2—i, c, m       5—k, y, c  
3—i, c            6—y, c  
                    7—A, y, c

INTERRUPT STATUS CODES

Class	INTERRUPT	Status Code Bits**									
		9	8	7	6	5	4	3	2	1	0
I	CP—Operand Memory Resume	0	0	0	0	0	0	0	0	0	0
I	CP—IOC Command Resume	0	0	0	0	0	0	0	0	0	0
I	CP—Instruction Memory Resume	0	0	0	0	0	0	0	0	0	0
I*	CP—IOC Interrupt Code Resume	0	0	0	0	0	0	0	0	0	1
I*	IOC Memory Resume	K	K	M	M	1	0	1	0	1	0
I*	Power/Interrupt Timeout	K	K	C	C	C	C	0	0	1	1
I*	Intercomple (never locked out)	0	0	0	0	0	0	1	1	1	1
II	Not Assigned	0	0	0	0	0	0	0	0	0	0
II	Characteristic Overflow	0	0	0	0	0	0	0	0	0	1
II	Characteristic Underflow	0	0	0	0	0	0	0	0	0	1
II	Floating Point Divide Error	0	0	0	0	0	0	0	0	0	1
II	Not Assigned	0	0	0	0	0	0	0	0	0	0
II	CP Illegal Instruction	0	1	0	0	0	0	0	0	0	0
II	Privileged Instruction Error	0	1	0	0	0	0	0	0	0	0
II	Not Assigned	0	0	0	0	0	0	0	0	0	0
II	Operand Breakpoint Match	1	0	0	0	0	0	0	0	0	0
II	Operand Read Lockout	1	0	0	0	0	0	0	0	0	0
II	Operand Write Lockout	1	0	0	0	0	0	0	0	0	0
II	Not Assigned	1	0	0	0	0	0	0	0	0	0
II	Instruction Breakpoint Match	1	0	0	0	0	0	0	0	0	0
II	Instruction Read Lockout	1	0	0	0	0	0	0	0	0	0
II*	CP Monitor Clock	1	1	1	1	1	1	1	1	1	1
III*	IOC Illegal CAR Instruction	K	K	0	0	0	0	0	0	0	0
III*	IOC Illegal Chain Instruction	K	K	C	C	0	0	1	0	0	0
III*	IOC Monitor Clock	K	K	0	0	0	0	0	0	0	1
III*	IOC CP Interrupt	K	K	0	0	0	0	0	0	0	1
III*	IOC External Interrupt Monitor	K	K	C	C	C	C	0	1	0	0
III*	IOC External Function Monitor	K	K	C	C	0	0	1	1	0	0
III*	IOC Output Data Monitor	K	K	C	C	C	C	0	0	0	0
III*	IOC Input Data Monitor	K	K	C	C	C	C	0	1	1	0

IV Executive Return 16 bit code assigned thru program  
\*Queued \*\*Definitions: PP—CPU NO. (0-2) FF—00—EXT. INT. MM/Ms—Memory Bank (0-17) 01—EXT. FCT. 10—OUTP. 11—OUTP. 12—OUTP. 13—OUTP. 14—OUTP. 15—OUTP. 16—OUTP. 17—OUTP. 18—OUTP. 19—OUTP. 20—OUTP. 21—OUTP. 22—OUTP. 23—OUTP. 24—OUTP. 25—OUTP. 26—OUTP. 27—OUTP. 28—OUTP. 29—OUTP. 30—OUTP. 31—OUTP. 32—OUTP. 33—OUTP. 34—OUTP. 35—OUTP. 36—OUTP. 37—OUTP. 38—OUTP. 39—OUTP. 40—OUTP. 41—OUTP. 42—OUTP. 43—OUTP. 44—OUTP. 45—OUTP. 46—OUTP. 47—OUTP. 48—OUTP. 49—OUTP. 50—OUTP. 51—OUTP. 52—OUTP. 53—OUTP. 54—OUTP. 55—OUTP. 56—OUTP. 57—OUTP. 58—OUTP. 59—OUTP. 60—OUTP. 61—OUTP. 62—OUTP. 63—OUTP. 64—OUTP. 65—OUTP. 66—OUTP. 67—OUTP. 68—OUTP. 69—OUTP. 70—OUTP. 71—OUTP. 72—OUTP. 73—OUTP. 74—OUTP. 75—OUTP. 76—OUTP. 77—OUTP. 78—OUTP. 79—OUTP. 80—OUTP. 81—OUTP. 82—OUTP. 83—OUTP. 84—OUTP. 85—OUTP. 86—OUTP. 87—OUTP. 88—OUTP. 89—OUTP. 90—OUTP. 91—OUTP. 92—OUTP. 93—OUTP. 94—OUTP. 95—OUTP. 96—OUTP. 97—OUTP. 98—OUTP. 99—OUTP. 100—OUTP. 101—OUTP. 102—OUTP. 103—OUTP. 104—OUTP. 105—OUTP. 106—OUTP. 107—OUTP. 108—OUTP. 109—OUTP. 110—OUTP. 111—OUTP. 112—OUTP. 113—OUTP. 114—OUTP. 115—OUTP. 116—OUTP. 117—OUTP. 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718—OUTP. 719—OUTP. 720—OUTP. 721—OUTP. 722—OUTP. 723—OUTP. 724—OUTP. 725—OUTP. 726—OUTP. 727—OUTP. 728—OUTP. 729—OUTP. 730—OUTP. 731—OUTP. 732—OUTP. 733—OUTP. 734—OUTP. 735—OUTP. 736—OUTP. 737—OUTP. 738—OUTP. 739—OUTP. 740—OUTP. 741—OUTP. 742—OUTP. 743—OUTP. 744—OUTP. 745—OUTP. 746—OUTP. 747—OUTP. 748—OUTP. 749—OUTP. 750—OUTP. 751—OUTP. 752—OUTP. 753—OUTP. 754—OUTP. 755—OUTP. 756—OUTP. 757—OUTP. 758—OUTP. 759—OUTP. 760—OUTP. 761—OUTP. 762—OUTP. 763—OUTP. 764—OUTP. 765—OUTP. 766—OUTP. 767—OUTP. 768—OUTP. 769—OUTP. 770—OUTP. 771—OUTP. 772—OUTP. 773—OUTP. 774—OUTP. 775—OUTP. 776—OUTP. 777—OUTP. 778—OUTP. 779—OUTP. 780—OUTP. 781—OUTP. 782—OUTP. 783—OUTP. 784—OUTP. 785—OUTP. 786—OUTP. 787—OUTP. 788—OUTP. 789—OUTP. 790—OUTP. 791—OUTP. 792—OUTP. 793—OUTP. 794—OUTP. 795—OUTP. 796—OUTP. 797—OUTP. 798—OUTP. 799—OUTP. 800—OUTP. 801—OUTP. 802—OUTP. 803—OUTP. 804—OUTP. 805—OUTP. 806—OUTP. 807—OUTP. 808—OUTP. 809—OUTP. 810—OUTP. 811—OUTP. 812—OUTP. 813—OUTP. 814—OUTP. 815—OUTP. 816—OUTP. 817—OUTP. 818—OUTP. 819—OUTP. 820—OUTP. 821—OUTP. 822—OUTP. 823—OUTP. 824—OUTP. 825—OUTP. 826—OUTP. 827—OUTP. 828—OUTP. 829—OUTP. 830—OUTP. 831—OUTP. 832—OUTP. 833—OUTP. 834—OUTP. 835—OUTP. 836—OUTP. 837—OUTP. 838—OUTP. 839—OUTP. 840—OUTP. 841—OUTP. 842—OUTP. 843—OUTP. 844—OUTP. 845—OUTP. 846—OUTP. 847—OUTP. 848—OUTP. 849—OUTP. 850—OUTP. 851—OUTP. 852—OUTP. 853—OUTP. 854—OUTP. 855—OUTP. 856—OUTP. 857—OUTP. 858—OUTP. 859—OUTP. 860—OUTP. 861—OUTP. 862—OUTP. 863—OUTP. 864—OUTP. 865—OUTP. 866—OUTP. 867—OUTP. 868—OUTP. 869—OUTP. 870—OUTP. 871—OUTP. 872—OUTP. 873—OUTP. 874—OUTP. 875—OUTP. 876—OUTP. 877—OUTP. 878—OUTP. 879—OUTP. 880—OUTP. 881—OUTP. 882—OUTP. 883—OUTP. 884—OUTP. 885—OUTP. 886—OUTP. 887—OUTP. 888—OUTP. 889—OUTP. 890—OUTP. 891—OUTP. 892—OUTP. 893—OUTP. 894—OUTP. 895—OUTP. 896—OUTP. 897—OUTP. 898—OUTP. 899—OUTP. 900—OUTP. 901—OUTP. 902—OUTP. 903—OUTP. 904—OUTP. 905—OUTP. 906—OUTP. 907—OUTP. 908—OUTP. 909—OUTP. 910—OUTP. 911—OUTP. 912—OUTP. 913—OUTP. 914—OUTP. 915—OUTP. 916—OUTP. 917—OUTP. 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Code	Mnemonic	NAME	DESCRIPTION	F	CA	R	UF	Time <sup>1</sup>
36	RAN	Replace Subtract	$Y \leftarrow (A_n) - (A_{n+1}); Y; (A_n) \leftarrow (A_n)$	I	Y	Y	1	2.5
37	RD	Replace Decrement	$Y \leftarrow (A_n) - 1; Y; (A_n) \leftarrow Y$	I	Y	Y	1	2.5
40	M	Multiply A	$(A_n) \cdot Y \rightarrow A_{n+1}; A_n$	I	Y	Y	1	7.5
41	D	Divide A	$(A_{n+1}, A_n) \cdot Y \rightarrow A_n$ ; remainder $\rightarrow A_{n+1}$	I	Y	Y	1	14.0
42	BC	Compare Bit to Zero	If $(Y)_{n-1} = 0$ , CD Set EQUAL If $(Y)_{n-1} = 1$ , CD Set UNEQUAL	I	N	Y	3	1.0
43	CXI	Compare Index Increment	If $(B)_n \geq Y$ , CD Set OUTSIDE; $0 \rightarrow B_n$ If $(B)_n < Y$ , CD Set WITHIN; $(B)_n \rightarrow B_n$	I	Y	Y	1	1.8
44	C	Compare A	Compare $(A)_n$ to $Y$ ; Set the CD	I	Y	Y	1	1.5
45	CL	Limit Compare A	If $(A_{n+1}) > Y$ , Set CD in Limit	I	Y	Y	1	1.5
46	CM	Mask Compare A	Compare $(A_{n+1})$ to $(A_n) \oplus Y$ ; Set the CD	I	Y	Y	1	1.5
47	CG	Gated Compare A	Compare $(A_n) \leftarrow (A_n) \oplus Y$ ; Set the CD	I	Y	Y	1	1.5
50	EPF	Jump on Even Parity	If $(A_{n+1}) \oplus (A_n)$ is Even Parity, JUMP to -Y	III	N	N	2,25	
50.1	JP	Jump on Odd Parity	If $(A_{n+1}) \oplus (A_n)$ is Odd Parity, JUMP to -Y	III	N	N	2,25	
50.2	DJZ	Jump Double Precision Zero	If $(A_{n+1}, A_n) = 0$ , JUMP to -Y	III	N	N	2,25	
50.3	DJNZ	Jump Double Precision Not Zero	If $(A_{n+1}, A_n) \neq 0$ , JUMP to -Y	III	N	N	2,25	
51.0	JP	Jump A Positive	If $(A_n) \geq 0$ , JUMP to -Y	III	N	N	1	1.5
51.1	JN	Jump A Negative	If $(A_n) < 0$ , JUMP to -Y	III	N	N	1	1.5
51.2	JZ	Jump A Zero	If $(A_n) = 0$ , JUMP to -Y	III	N	N	1	1.5
51.3	JNZ	Jump A Not Zero	If $(A_n) \neq 0$ , JUMP to -Y	III	N	N	1	1.5
52.0	LBJ	Load B and Jump	$P + 1 \rightarrow B_n$ ; JUMP to -Y	III	N	N	1	1.8
52.1	JBNZ	Jump B Not Zero	If $(B)_n \neq 0$ , then $(B)_n \rightarrow B_n$ ; JUMP to -Y	III	N	N	1	1.8
52.2	JS	JUMP to $Y + (B)_n$	JUMP to $Y + (B)_n$	III	N	13		
52.3	JL	Unconditional Jump Lower	JUMP to the Lower of -Y	III	N	12		1.5
53.0=a-0	JNF	Jump on Overflow	If OD is not Set, JUMP to -Y; Clear OD	III	N	12		1.5
53.0=a-1	OF	Overflow	If OD is Set, JUMP to -Y; Clear OD	III	N	12		1.5
53.0=a-2	JNE	Jump on Not Equal	If CD $\neq$ , JUMP to -Y	III	N	12		1.5
53.1=a-1	JE	Jump on Equal	If CD =, JUMP to -Y	III	N	12		1.5
53.1=a-2	JG	Jump on Greater Than	If $CD >$ , JUMP to -Y	III	N	12		1.5
53.1=a-3	JGE	Jump on Greater Than or Equal	If $CD \geq$ , JUMP to -Y	III	N	12		1.5
53.1=a-4	JLT	Jump on Less Than	If $CD <$ , JUMP to -Y	III	N	12		1.5
53.1=a-5	JLE	Jump on Less Than or Equal	If $CD \leq$ , JUMP to -Y	III	N	12		1.5
53.1=a-6	JNW	Jump Outside Limits	If CD Outside Limits, JUMP to -Y	III	N	12		1.5
53.1=a-7	JW	Jump Within Limits	If CD Within Limits, JUMP to -Y	III	N	12		1.5
53.2	RJ	Return Jump	$P_n \rightarrow Y$ ; JUMP to $Y - 1$	III	N	12		3.0
53.3	RJ	Return Jump	If switch a is Set, $P_n \rightarrow Y$ ; JUMP to $Y - 1$	III	N	12		3.0
53.3*	RJC	Return Jump	$P_n \rightarrow Y$ ; JUMP to $Y - 1$ ; if switch a is Set, $P_n \rightarrow Y$	III	N	12		3.0
53.3	J	Manual Jump	JUMP to -Y	III	N	1		3.0
53.3	JC	Manual Jump	If switch a is Set, JUMP to -Y	III	N	12		1.5
53.3*	JSC	Manual Jump	JUMP to -Y if switch a is Set, Stop	III	N	1		1.5
54	LCT	Load CMR (task)	$Y \leftarrow CMR_n$	I	Y	3		1.5
55	LCI	Load CMR (interrupt)	$Y \leftarrow CMR_{n+10}$	I	Y	3		1.5
56	SC	Store CMR (task)	$CMR_n \rightarrow Y$	I	Y	3		1.5
57	SCT	Store CMR (interrupt)	$CMR_{n+10} \rightarrow Y$	I	Y	3		1.5
60 <sub>1</sub> =I=0	NSCT	Store CMR in Ab (task)	$CMR_{n+10} \rightarrow Ab$	IV	N	4		15.1,5
60 <sub>1</sub> =I=1	NSC	Store CMR in Ab (interrupt)	$CMR_n \rightarrow Ab$	IV	N	4		15.1,5
61 <sub>1</sub> =I=0	HLCT	Load CMR with Ab (task)	$(Ab) \rightarrow CMR_n$	IV	N	4		15.1,5
61 <sub>1</sub> =I=1	HLCI	Load CMR with Ab (interrupt)	$(Ab) \rightarrow CMR_{n+10}$	IV	N	4		15.1,5
62	NLC	Shift Left Circular	Left Shift Circular	IV	N	11		1.8,1.8
63	NLDC	Left Double Shift Circular	Left Double Shift Circular	IV	N	11		1.8,1.8
64	HRZ	Shift Right Zero Fill	Right Shift Zero Fill	IV	N	11		1.8,1.8
65	HRDZ	Shift Right Double Zero Fill	Right Double Shift Zero Fill	IV	N	11		1.8,1.8
66	HRS	Shift Right Sign Filled	Right Shift Sign Filled	IV	N	11		1.8,1.8
67	HRDS	Shift Double Right Sign Filled	Right Double Shift Sign Filled	IV	N	11		1.8,1.8
70.0	HSF	Single Scale Factor A	Normalize $(A_n)$ Shift Count $\rightarrow Ab$	IV	N	5		20.2,0
70.1	HSDF	Double Scale Factor A	Normalize $(A_{n+1}, A_n)$ Shift Count $\rightarrow Ab$	IV	N	5		20.2,0
70.2	HCP	Complement A	$(A_n) \rightarrow A_n$	IV	N	7		15.1,5
70.3	HDCP	Double Complement A	$(A_{n+1}, A_n) \rightarrow A_{n+1}, A_n$	IV	N	7		15.1,5
71.0	HOR	Inclusive OR A	$(A_n) \oplus (Ab); (A_n); (Ab)$	IV	N	5		15.7,5
71.1	HA	Sum	$(A_n) \oplus (Ab) \rightarrow A_n$	IV	N	5		15.7,5
71.2	HAN	Difference	$(A_n) - (Ab) \rightarrow A_n$	IV	N	5		15.7,5
71.3	HXOR	Exclusive OR A	$(A_n) \oplus (Ab) \rightarrow A_n$	IV	N	5		15.7,5
71.5	HAND	AND A	$(A_n) \oplus (Ab); (A_n); (Ab)$	IV	N	5		15.7,5
74.0	HM	Mask	$(A_n) \oplus (Ab) \rightarrow A_n$	IV	N	7		15.7,5
74.1	HD	Divide	$(A_{n+1}, A_n) \rightarrow (Ab)$ ; Remainder $\rightarrow A_{n+1}$	IV	N	5		14.0,14.0
74.2	HRT	Square Root	$\sqrt{(A_{n+1}, A_n)} \rightarrow Ab$ ; Residue $\rightarrow A_{n+1}$	IV	N	5		15.0,15.0
74.3	ALB	Load Ba with Bb	$(Bb) \rightarrow Ba$	IV	N	5		15.1,1.0
74.4	NC	Compare As with Ab	Compare $(A_n)$ to $(Ab)$ ; Set CD	IV	N	5		15.1,0
74.5	NCL	Limit Compare (register)	If $(A_{n+1}) > (Ab)$ , Set CD in Limit	IV	N	5		15.1,0
74.6	NCM	Mask Compare (register)	Compare $(A_{n+1}) \oplus (A_n)$ to $(Ab)$ ; Set the CD	IV	N	5		15.1,0
74.7	NCB	Compare (Bb) to (Ba); Set the CD	Compare $(B_n)$ to $(B_{n+1})$ ; Set the CD	IV	N	5		15.1,1.5
77.0**	HSIM	Read I/O Monitor Clock	(IOCA MON CLK) $\rightarrow Ab$	IV	N	5		3.0,3.0
77.1**	HSRD	Read Real Time Clock	(IOCA RTC) $\rightarrow Ab$	IV	N	5		3.3,3.5
77.4**	HPI	Prevent Class III Interrupts	Set Class III Interrupt Lockout	IV	N	9		2.25,2.25
77.5**	HAI	Allow Class III Interrupts	Clear Class III Interrupt Lockout	IV	N	9		2.25,2.25
77.6**	HAI	Stop	Clear CPU	IV	N	9		1.5,1.5

<sup>1</sup>Privileged \*\*CPU=IOC Instr.—Privileged  
<sup>2</sup>Privileged when  $a_n=6x$  or  $7x$   
 21.5 is memory with operands not in same bank as instructions (overlapped).  
 1.5,1.5 indicates time for instruction when in upper half/lower half word.

ULTRA PARAMETER FORMATS (UF)

No.	Parameter	No.	Parameter	No.	Parameter
1	$a, k, b, s$	6	$a, sy, b$	11	$a, m$ (shift by $m$ )
2	$a, y, b, s$	7	$a, b, s$		$a, b, 1$ (shift by $B_n$ )
3	$ak, y, b, s$	8	$y, b, s$		$a, b, 2$ (shift by $B_n$ )
4	$a, b, s$	9	None	12	$y, k, b, s$
5	$a, b$	10	$sy, b$	13	$y, k, b$

Asterisk (\*) preceding  $y$  indicates indirect address

INSTRUCTION WORD FORMATS

Format I

31	26	25	23	22	20	19	17	16	15	13	12	0
f	a	k	b	i	s	y						

Format II

31	26	25	23	22	20	19	17	16	15	13	12	0
f	a	t <sub>2</sub>	b	i	s	y						

Format III

31	26	25	23	22	21	20	19	17	16	15	13	12	0
f	a	t <sub>2</sub>	k	b	i	s	y						

CENTRAL PROCESSOR CONTROL MEMORY ADDRESS ASSIGNMENT

Address	Use	Bits
0-7	Accumulator (A) registers 0-7	32
10	Unassigned	18
11-17	Index (B) registers 1-7	18
20-27	Base (S) registers 0-7	18
30-57	Unassigned (not usable)	18

Interrupt Mode

Address	Use	Bits
6x	Breakpoint register	20
7x	Active status register	32
100-107	Accumulator (A) registers 0-7	32
110	CP monitor clock register	18
111-117	Index (B) registers 1-7	18
120-127	Base (S) registers 0-7	18
130-137	Unassigned (not usable)	18
140	ICW—Class I	18
141	DSW—Class I ASR storage	18
142	DSW—Class I interrupt status code	18
143	DSW—Class I P—storage	18
144	ICW—Class II	18
145	DSW—Class II ASR storage	18
146	DSW—Class II interrupt status code	18
147	DSW—Class II P—storage	18
150	ICW—Class III	18
151	DSW—Class III ASR storage	18
152	DSW—Class III interrupt status code	18
153	DSW—Class III P—storage	18
154	ICW—Class IV	18
155	DSW—Class IV ASR storage	18
156	DSW—Class IV interrupt status code	18
157	DSW—Class IV P—storage	18
166-177	MIO—registers for banks 0-15	16

Form IV A Form IV B

15	10	9	7	6	4	3	1	0
f	a	t <sub>2</sub>	b	i	s	y		

INDIRECT ADDRESS WORD FORMAT

31	30	29	25	24	20	19	17	16	15	13	12	0
c	w	b										

1—Function Code  
 f<sub>1</sub>—Subfunction Code  
 a—Accumulator Register  
 k—Operand Interpretation  
 b—Index Register  
 i—Indirect Bit  
 s—Function  
 y—Operand Address  
 m—Shift Designator

Bit 2<sup>1</sup>

1—Shift by count 2<sup>n</sup>  
 0—1 Shift by 1  
 0—Single Character  
 1—Sequential Character  
 b is specified by bits 2<sup>1</sup>-2<sup>2</sup>

FORMAT I INSTRUCTION k—FIELD INTERPRETATION

k	Memory to Arithmetic (Read)	Arithmetic to Memory (Store)
0	$Y \leftarrow (B_n) \rightarrow A_n$ SE	Not Used
1	$(A_n) \rightarrow (B_n)$ SE	$Y \rightarrow A_n$
2	$(A_n) \rightarrow A_{n+1}$ SE	$(A_n) \rightarrow Y_{n+1}$
3	$(Y) \rightarrow A_n$ SE	$(A_n) \rightarrow Y_n$
4	$(Y) \rightarrow A_{n+1}$ SE	$(A_n) \rightarrow Y_{n+1}$
5	$(A_n) \rightarrow A_n$ ZE	$Y \rightarrow A_n$
6	$(Y) \rightarrow A_n$ ZE	$(A_n) \rightarrow Y_{n+1}$
7	$(Y) \rightarrow A_{n+1}$ ZE	$(A_n) \rightarrow Y_{n+1}$

k—Field Interpretation for Replace Instructions:  
 Read Cycle—Same as memory to arithmetic.  
 Store Cycle—Same as arithmetic to memory.  
 SE—Sign Extended; ZE—Zero Extended; U—Unchanged

REPEAT CONDITIONS

a	Non-Compare Instructions	a	Compare Instructions
0	Terminate if A $\neq$ 0	0	Terminate if CD set to $\neq$
1	Terminate if A = 0	1	Terminate if CD set to =
2	Terminate if A $>$ 0	2	Terminate if CD set to $>$
3	Terminate if A $<$ 0	3	Terminate if CD set to $<$
4	Do not terminate	4	Terminate if CD set to $\geq$
5	Terminate if (A) is even parity on write into memory	5	Terminate if CD set to $\leq$
6	Terminate if (A) is odd parity on write into memory	6	Terminate if CD set to Outside limit
7	Do not terminate	7	Terminate if CD set to within limit

FLOATING POINT FORMAT (each word is one's complement)

Sign Flag	= 14	0	$\pm$ 30	0
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Characteristic(exponent) in  $A_n$  or  $Y$   
 Mantissa in  $A_{n+1}$  or  $Y+1$

MEMORY LOCKOUT REGISTER

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0

Set—Read locked out  
 Set—Write locked out  
 0 0 0 0 — 0-37777  
 0 4 0 0 0 — 0-77777  
 0 0 0 0 0 — 1-37777  
 1 4 0 0 0 — 1-77777  
 2 0 0 0 0 — 2-37777  
 3 0 0 0 0 — 2-77777  
 3 4 0 0 0 — 3-37777  
 3 4 0 0 0 — 3-77777

BREAKPOINT REGISTER

19	18	17
0		