THE NEXT GENERATION

The U.S. Navy's newest "next generation" computer is now ready for service. Built by Univac Federal Systems Division, under the sponsorship of the Naval Ship Engineering Center, the AN/UYK-7(V) computer represents a major advancement in real-time data processing.

Designed to cope with the increasing complexity of modern shipboard operations, AN/UYK-7(V) is a reliable, general purpose, high performance computer — adaptable to a wide variety of real-time data processing applications. These applications include signal processing, command and decision, control and information systems.

The AN/UYK-7(V) combines the advantages of modular "building block" construction and microelectronic integrated circuits to provide higher reliability ... faster processing speeds ... and greater data processing capabilities than any militarized computer presently in service. Yet the AN/UYK-7(V) is smaller in physical size, weighs less, and has a lower power consumption than the normal large scale digital computer. Through the use of this unique, modular "building block" design concept, the AN/UYK-7(V) provides for ease of system expansion and adaptation to changing mission requirements.

Whether your requirements emphasize large, high speed input/output capability, multi-processing capability or large memory capacity, the AN/UYK-7(V) can be adapted to your needs. Updating the system for meeting future changing environmental and operational requirements is possible without extensive computer re-design. Expansion is achieved by adding only those modules necessary for providing the required functions.

The AN/UYK-7(V) multi-processing capabilities, combined with memory sharing by both the processors and the input/output controllers, plus memory overlap and interleaving features, allows an economic selection of modules to process more data in much shorter time and with much less hardware.

In the past, shipboard operational conditions may have required three or more separate or different unit computers to perform the various data processing tasks, thus compounding problems in equipment standardization, maintenance and logistics. The compact AN/UYK-7(V) modularized computer offers the opportunity to standardize all shipboard digital computers for increased system reliability — thus reducing the costs normally incurred in maintaining extensive multi-computer parts inventories, training and repair facilities.

The AN/UYK-7(V) computer represents a refinement of the unit computers presently operating aboard ships of the fleet. It is designed to meet the Navy's expanded electronic data processing plans, and enables a new concept of tactical planning through its large scale, real-time data processing capabilities.

HISTORY

Development of the AN/UYK-7(V) Digital Data Computer System began in December 1967 when the Naval Ship Systems Command awarded its initial contract to Univac.

As a major supplier of data processing systems and sub-systems to the Department of Defense and other government agencies, Univac Federal Systems Division has maintained close contact with the various U.S. Navy Commands which are involved in the development of digital systems.

Over the years, Univac has provided maximum interchange of technical and management information with the Navy through regular briefings on Univac activities and participation by Univac personnel at symposiums and technical sessions sponsored by Navy organizations.

Through this active interchange of information, Univac has become knowledgeable of the many requirements and problems existing in the development of tactical data systems. This knowledge, in addition to Univac's long record of experience in building computers for the Navy, assures the successful completion of the AN/UYK-7(V) program and the future systems it will serve.
Figure 1 shows a typical configuration of a "unit computer." The central processor module controls the timing of the entire unit. When one portion — processor, memory or input-output controller — is operating, the others must wait for completion to continue their operation. This concept causes many problems in various applications. The "unit computer," because it was designed specifically for a particular application, is not general purpose enough to be used most efficiently for other applications such as weapons control and signal processing.

To solve these applications problems, the Navy considered several solutions. The first, a "compromise computer," would include only the features needed for satisfying each application. The disadvantage of this approach is that none of the applications systems would operate in its most efficient mode. Another approach, the "super-computer," would consist of a large scale computer capable of solving all applications problems. However, by its very size, its cost would be excessive for initial installation.

The final solution, and the solution used in the design of the AN/UYK-7(V), is the "building-block" concept. This modular concept places complete functional sections within independent modules. To provide maximum versatility, the processor, memory and input-output controller modules communicate with each other on a request and acknowledge basis.

As shown in figure 2, each module operates independently under its own control. A prime advantage of this design is that it provides for easy adaptation to changing operational and mission requirements. Thus, an initial AN/UYK-7(V) installation can be economically expanded in the field to meet newer and larger requirements through easy "add on" of needed modules. By the nature of the modular "building-block" design, special purpose equipment can be attached to standard interfaces.

**GENERAL CHARACTERISTICS**

The AN/UYK-7(V), because of its design, provides for multi-processing and shared-memory operation. All the features required for an efficient multi-processing system are designed into the AN/UYK-7(V).

The instruction repertoire of the AN/UYK-7(V) is extensive, providing separate hardware functions for double-precision fixed-point and floating-point arithmetic, as well as the many special functions required for multi-processing.

The central processor cycle time is 750 nanoseconds, and the memory module cycle time is 1.5 microseconds. In addition to the basic hardware speeds, several program operational advantages can be gained through the unique design features, such as multiple state operation, which provides the user with a sophisticated system of interrupt levels; processor overlapping and interleaving of memory banks, which avoids conflicts in time memory shared systems; and command
chaining of I/O controller instructions, which provides system advantages in repetitive I/O operations through parallel operation with the central processor.

Optional electrical interface capabilities (NTDS FAST, SLOW, A-NEW, and SERIAL) combined with the ability to handle parallel slow, fast and/or serial data transmissions permit the AN/UYK-7(V) to operate with most presently used external data sources.

The AN/UYK-7(V) has been designed to provide maximum reliability. The mean-time-between-failure is 2000 hours, for the basic system. The mean-time-to-repair is 15 minutes. Components, and packaging techniques, are military approved.

**EXPANSION CHARACTERISTICS**

The AN/UYK-7(V) computer is configured from the following modules, as required:
- Central Processor
- Input/Output (I/O) Controller
- Input/Output (I/O) Adapter, 4, 8, 12 or 16 I/O Channels)
- 16K Word Memory (16,384 32-bit words)
- Power Supply

The AN/UYK-7(V) modular design concept eliminates many of the system limiting factors imposed by present-day unit computers.

Expansion limits are determined only by the amount of inter-module communication required and the addressing capability of each module. Each central processor uses two memory accesses and each I/O controller uses one access.

The central processor module can communicate with four input-output controllers, and up to 16 memory modules. The memory modules each have eight accesses. The input-output controller communicates through an input-output adapter to 16 channels. It also can communicate with three central processor modules and up to 16 memory modules.

**EXPANSION CAPABILITIES**

Modular multi-point connections, combined with asynchronous operation of the central processor, memory and I/O controller components permit a wide variety of computer configurations. Typical large-scale AN/UYK-7(V) configurations having multiple central processors, I/O controllers and shared memory units can include:

**TWO CENTRAL PROCESSOR MODULES**
- Four I/O controller modules
- Four I/O adapter modules (64 I/O channels)
- Sixteen memory modules (262,144 32-bit words)
- Five power supply modules
- Two maintenance consoles

**THREE CENTRAL PROCESSOR MODULES**
- Two I/O controller modules
- Two I/O adapter modules (32 I/O channels)
- Sixteen memory modules (262,144 32-bit words)
- Five power supply modules
- Three maintenance consoles
APPLICATIONS

The AN/UYS-7(V) has been designed to operate flexibly in many distinct applications. In the total environment, such as a ship, there are many diverse operations. These include sensor processing, weapons control, logistics and over-all command and decision. Following is a brief description of these applications, as they are handled by the AN/UYS-7(V) computer.

Radar Signal Processing

A major shipboard application is that of signal processing. In this application, radar, beacon, sonar, and those signals used in electronic warfare, must be processed and acted upon in a minimum of time. Radar applications provide a continual input of data in a real-time environment. This requires a great deal of processing in order to determine targets, direction, and other information. The combination of this large amount of data, and the complex processing required, places an enormously large load on the computer. In the AN/UYS-7(V), the real-time data processing task is handled easily due to the fast, independent operation of the modular functional sections, the high speed memory and fast central processing cycle time, as well as the very large and comprehensive instruction repertoire which allows computations to be performed in a high speed real-time mode. The handling of input data in a real-time response is accomplished by the very fast input-output section, which can be expanded by additional input-output controllers and input-output adapter modules if they are required.

Weapons Control Systems

In addition to weapons control systems, other control systems normally found on board ship include air traffic, radar, electronic countermeasures, and navigational control systems. Complex weapons control systems, as with signal processing applications, require high computational capabilities in the central processor. While the quantity of input data is lower, input is received from more than one source. Once again, the AN/UYS-7(V) is uniquely qualified for this application since the number of input-output channels can be expanded to the number necessary for the multiple input data. In addition, the complex computation required for swiftly determining directional commands for the weapons is easily accomplished with the floating-point arithmetic feature, double-precision hardware, multiple accumulators, and by the 750 nanosecond speed of the central processor.

Information Systems

Logistics, intelligence control, communications and other management information is an additional problem to be solved. In this area, the operational requirements are for accepting and storing a very large amount of data, providing minimum computation on this data, and then directing selected amounts of it to various command sources. The modular memory feature suits this application quite well in that additional memory components can be added to accept a large store of data. The reduction and selective communication of this data can be handled by the AN/UYS-7(V) through use of its flexible input-output structure. The memory protect feature allows isolation of data and insures against access to data by unauthorized personnel.

Command and Decision Systems

All of these different applications are combined within a total command and decision network. Here again, rather than using a different computer, the AN/UYS-7(V) can be structured to provide those features unique to the command and decision requirements. Because of the modular capabilities, the user does not require different computers because the AN/UYS-7(V) functions in itself as a whole family of computers, meeting each specific requirement.
### AN/UYK-7(V)
#### CENTRAL PROCESSOR INSTRUCTION REPERTOIRE

<table>
<thead>
<tr>
<th>Octal Code</th>
<th>Mnemonic Code</th>
<th>Name</th>
<th>Overlapped Execution Time (μ sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 0</td>
<td>OR</td>
<td>Inclusive OR</td>
<td>1.5</td>
</tr>
<tr>
<td>01 1</td>
<td>SC</td>
<td>Selective Clear</td>
<td>1.5</td>
</tr>
<tr>
<td>01 2</td>
<td>MS</td>
<td>Masked Selective Substitute</td>
<td>1.5</td>
</tr>
<tr>
<td>01 3</td>
<td>XOR</td>
<td>Exclusive OR</td>
<td>1.5</td>
</tr>
<tr>
<td>01 4</td>
<td>ALP</td>
<td>Add Logical Product</td>
<td>1.5</td>
</tr>
<tr>
<td>01 5</td>
<td>LLP</td>
<td>Load Logical Product</td>
<td>1.5</td>
</tr>
<tr>
<td>01 6</td>
<td>NLP</td>
<td>Add Negative Logical Product</td>
<td>1.5</td>
</tr>
<tr>
<td>01 7</td>
<td>LLPN</td>
<td>Load Logical Product Next</td>
<td>1.5</td>
</tr>
<tr>
<td>02 0</td>
<td>CMH</td>
<td>Count Ones</td>
<td>7.5</td>
</tr>
<tr>
<td>02 2</td>
<td>XR</td>
<td>Execute Remote</td>
<td>1.5</td>
</tr>
<tr>
<td>02 3</td>
<td>XRL</td>
<td>Execute Remote Lower</td>
<td>1.5</td>
</tr>
<tr>
<td>02 4</td>
<td>SLR</td>
<td>Store Logical Product</td>
<td>2.5</td>
</tr>
<tr>
<td>02 5</td>
<td>SSM</td>
<td>Store Sum</td>
<td>2.5</td>
</tr>
<tr>
<td>02 6</td>
<td>SDIF</td>
<td>Store Difference</td>
<td>2.5</td>
</tr>
<tr>
<td>02 7</td>
<td>DS</td>
<td>Double Store A</td>
<td>3.0</td>
</tr>
<tr>
<td>03 0</td>
<td>ROR</td>
<td>Replace Inclusive OR</td>
<td>2.5</td>
</tr>
<tr>
<td>03 1</td>
<td>RSC</td>
<td>Replace Selective Clear</td>
<td>2.5</td>
</tr>
<tr>
<td>03 2</td>
<td>RNS</td>
<td>Masked Selective Substitute</td>
<td>2.5</td>
</tr>
<tr>
<td>03 3</td>
<td>RXOR</td>
<td>Replace Exclusive OR</td>
<td>2.5</td>
</tr>
<tr>
<td>03 4</td>
<td>RALP</td>
<td>Replace Add Logical</td>
<td>2.5</td>
</tr>
<tr>
<td>03 5</td>
<td>RLP</td>
<td>Replace Logical Product</td>
<td>2.5</td>
</tr>
<tr>
<td>03 6</td>
<td>RNLP</td>
<td>Replace Negative Logical Product</td>
<td>2.5</td>
</tr>
<tr>
<td>03 7</td>
<td>TSF</td>
<td>Test and Set Flag</td>
<td>2.5</td>
</tr>
<tr>
<td>05 0</td>
<td>DLI</td>
<td>Double Load A</td>
<td>3.0</td>
</tr>
<tr>
<td>05 1</td>
<td>DA</td>
<td>Double Add A</td>
<td>3.0</td>
</tr>
<tr>
<td>05 2</td>
<td>DANT</td>
<td>Double Add Negative A</td>
<td>3.0</td>
</tr>
<tr>
<td>05 3</td>
<td>DC</td>
<td>Double Compare A</td>
<td>3.0</td>
</tr>
<tr>
<td>06 0</td>
<td>FA</td>
<td>Floating Point Add</td>
<td>6.0</td>
</tr>
<tr>
<td>06 1</td>
<td>FAN</td>
<td>Floating Point Add Negative</td>
<td>6.0</td>
</tr>
<tr>
<td>06 2</td>
<td>FAM</td>
<td>Floating Point Multiply</td>
<td>10.0</td>
</tr>
<tr>
<td>06 3</td>
<td>FD</td>
<td>Floating Point Divide</td>
<td>16.0</td>
</tr>
<tr>
<td>06 4</td>
<td>FDR</td>
<td>Floating Point Add Round</td>
<td>6.0</td>
</tr>
<tr>
<td>06 5</td>
<td>FANR</td>
<td>Floating Point Add Multiply</td>
<td>6.0</td>
</tr>
<tr>
<td>06 6</td>
<td>FMR</td>
<td>Floating Point Multiply Round</td>
<td>10.0</td>
</tr>
<tr>
<td>06 7</td>
<td>FDRR</td>
<td>Floating Point Divide Round</td>
<td>16.0</td>
</tr>
<tr>
<td>07 0</td>
<td>XE</td>
<td>Enter Executive State</td>
<td>3.0</td>
</tr>
<tr>
<td>07 1</td>
<td>AEI</td>
<td>Allow Interrupt</td>
<td>3.0</td>
</tr>
<tr>
<td>07 2</td>
<td>RII</td>
<td>Prevent Interrupt</td>
<td>3.0</td>
</tr>
<tr>
<td>07 3</td>
<td>LIM</td>
<td>Load, Enable I/O Monitor Clock</td>
<td>3.0</td>
</tr>
<tr>
<td>07 4</td>
<td>IO</td>
<td>Initiate I/O</td>
<td>3.0</td>
</tr>
<tr>
<td>07 5</td>
<td>IR</td>
<td>Interrupt Return</td>
<td>3.0</td>
</tr>
<tr>
<td>07 6</td>
<td>RP</td>
<td>Repeat</td>
<td>3.0</td>
</tr>
<tr>
<td>08 0</td>
<td>LA</td>
<td>Load A</td>
<td>1.5</td>
</tr>
<tr>
<td>08 1</td>
<td>LAX</td>
<td>Load A and Index B</td>
<td>1.5</td>
</tr>
<tr>
<td>08 2</td>
<td>LDY</td>
<td>Load Y A</td>
<td>1.5</td>
</tr>
<tr>
<td>08 3</td>
<td>ANA</td>
<td>Add Negative A</td>
<td>1.5</td>
</tr>
<tr>
<td>08 4</td>
<td>AAT</td>
<td>Add A</td>
<td>1.5</td>
</tr>
<tr>
<td>08 5</td>
<td>LSUM</td>
<td>Load Y A</td>
<td>1.5</td>
</tr>
<tr>
<td>08 6</td>
<td>LNA</td>
<td>Load Negative A</td>
<td>1.5</td>
</tr>
<tr>
<td>08 7</td>
<td>LM</td>
<td>Load Magnitude A</td>
<td>1.5</td>
</tr>
<tr>
<td>09 0</td>
<td>LB</td>
<td>Load B</td>
<td>1.5</td>
</tr>
<tr>
<td>09 1</td>
<td>AB</td>
<td>Add B</td>
<td>1.8</td>
</tr>
<tr>
<td>09 2</td>
<td>ANB</td>
<td>Add Negative B</td>
<td>1.8</td>
</tr>
<tr>
<td>09 3</td>
<td>SB</td>
<td>Store B</td>
<td>1.5</td>
</tr>
<tr>
<td>09 4</td>
<td>SA</td>
<td>Store A</td>
<td>1.5</td>
</tr>
<tr>
<td>09 5</td>
<td>SAB</td>
<td>Store A and Index B</td>
<td>1.5</td>
</tr>
<tr>
<td>09 6</td>
<td>SNA</td>
<td>Store Negative A</td>
<td>1.5</td>
</tr>
<tr>
<td>09 7</td>
<td>SM</td>
<td>Store Magnitude A</td>
<td>1.5</td>
</tr>
<tr>
<td>0A 0</td>
<td>BZ</td>
<td>Clear Bit</td>
<td>2.5</td>
</tr>
<tr>
<td>0A 1</td>
<td>BS</td>
<td>Set Bit</td>
<td>2.5</td>
</tr>
<tr>
<td>0A 2</td>
<td>RA</td>
<td>Replace Add</td>
<td>2.5</td>
</tr>
<tr>
<td>0A 3</td>
<td>RR</td>
<td>Replace Increment</td>
<td>2.5</td>
</tr>
<tr>
<td>0A 4</td>
<td>RAN</td>
<td>Replace Add Negative</td>
<td>2.5</td>
</tr>
<tr>
<td>0A 5</td>
<td>RD</td>
<td>Replace Decrement</td>
<td>2.5</td>
</tr>
<tr>
<td>0A 6</td>
<td>M</td>
<td>Multiply</td>
<td>7.5</td>
</tr>
<tr>
<td>0A 7</td>
<td>D</td>
<td>Divide</td>
<td>1.4</td>
</tr>
<tr>
<td>0B 0</td>
<td>BC</td>
<td>Compare Bit to Zero</td>
<td>1.5</td>
</tr>
<tr>
<td>0B 1</td>
<td>CXI</td>
<td>Compare Index Increment</td>
<td>1.8</td>
</tr>
<tr>
<td>0B 2</td>
<td>C</td>
<td>Compare A</td>
<td>1.5</td>
</tr>
<tr>
<td>0B 3</td>
<td>CL</td>
<td>Limit Compare A</td>
<td>1.5</td>
</tr>
<tr>
<td>0B 4</td>
<td>CM</td>
<td>Masked Compare A</td>
<td>1.5</td>
</tr>
</tbody>
</table>

*High value when instruction is in upper half of word; low value when instruction is in lower half of word.

### I/O CONTROLLER COMMANDS

<table>
<thead>
<tr>
<th>Octal Code</th>
<th>Mnemonic Code</th>
<th>Name</th>
<th>Overlapped Execution Time (μ sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 0</td>
<td>IB</td>
<td>Initiate Input Buffer on Cj</td>
<td>3.25</td>
</tr>
<tr>
<td>01 1</td>
<td>OB</td>
<td>Initiate Output Buffer on Cj</td>
<td>3.25</td>
</tr>
<tr>
<td>01 2</td>
<td>EB</td>
<td>Initiate EF Buffer on Cj</td>
<td>3.25</td>
</tr>
<tr>
<td>01 3</td>
<td>XE</td>
<td>Initiate EI Buffer on Cj</td>
<td>3.25</td>
</tr>
<tr>
<td>01 4</td>
<td>TIB</td>
<td>Terminate Input Buffer on Cj</td>
<td>3.0</td>
</tr>
<tr>
<td>01 5</td>
<td>TOB</td>
<td>Terminate Output Buffer on Cj</td>
<td>3.0</td>
</tr>
<tr>
<td>01 6</td>
<td>TFBI</td>
<td>Terminate EF Buffer on Cj</td>
<td>3.0</td>
</tr>
<tr>
<td>01 7</td>
<td>TXBI</td>
<td>Terminate EI Buffer on Cj</td>
<td>3.0</td>
</tr>
<tr>
<td>02 0</td>
<td>OMIR</td>
<td>Set Input Monitor Interrupt Request on Cj</td>
<td>2.5</td>
</tr>
<tr>
<td>02 1</td>
<td>FMR</td>
<td>Set EF Monitor Interrupt Request on Cj</td>
<td>2.5</td>
</tr>
<tr>
<td>02 2</td>
<td>XMIR</td>
<td>Set EI Monitor Interrupt Request on Cj</td>
<td>2.5</td>
</tr>
<tr>
<td>02 3</td>
<td>AFC</td>
<td>Set EF Chain Active on Cj</td>
<td>2.5</td>
</tr>
<tr>
<td>02 4</td>
<td>AXC</td>
<td>Set EI Chain Active on Cj</td>
<td>2.5</td>
</tr>
<tr>
<td>02 5</td>
<td>TBZ</td>
<td>Test for Bit Not Set</td>
<td>4.0</td>
</tr>
<tr>
<td>02 6</td>
<td>TBS</td>
<td>Test for Bit Set</td>
<td>4.0</td>
</tr>
<tr>
<td>02 7</td>
<td>JIO</td>
<td>Jump Command to Y</td>
<td>2.5</td>
</tr>
<tr>
<td>02 8</td>
<td>LICT</td>
<td>Load Control Memory</td>
<td>3.25</td>
</tr>
<tr>
<td>02 9</td>
<td>LRPC</td>
<td>Load RTC</td>
<td>4.0</td>
</tr>
<tr>
<td>02 A</td>
<td>SICM</td>
<td>Store Control Memory</td>
<td>2.75</td>
</tr>
<tr>
<td>02 B</td>
<td>IB</td>
<td>Set Bit</td>
<td>3.25</td>
</tr>
<tr>
<td>02 C</td>
<td>IBZ</td>
<td>Clear Bit</td>
<td>3.25</td>
</tr>
<tr>
<td>02 D</td>
<td>BTST</td>
<td>Test and Set Flag</td>
<td>3.25</td>
</tr>
</tbody>
</table>

*16k = 16384, *2k = 4096
AN/UYK-7(V) DIGITAL COMPUTER SPECIFICATIONS

RANGE OF CAPABILITY

• MINIMUM
  ONE PROCESSOR MODULE
  ONE INPUT/OUTPUT CONTROLLER MODULE
  ONE INPUT/OUTPUT ADAPTER MODULE (4 CHANNELS)
  ONE MEMORY MODULE (16,384 WORDS)
  ONE POWER SUPPLY MODULE

• TYPICAL LARGE
  THREE PROCESSOR MODULES
  TWO INPUT/OUTPUT CONTROLLER MODULES
  TWO INPUT/OUTPUT ADAPTER MODULES (32 CHANNELS)
  SIXTEEN MEMORY MODULES (262,144 WORDS)
  FIVE POWER SUPPLY MODULES

FUNCTIONAL

• CENTRAL PROCESSOR
  GENERAL PURPOSE, PARALLEL, BINARY
  FLEXIBLE BASE AND INDEX ADDRESSING
  CASCaded INDIRECT ADDRESSING
  REPERTOIRE OF 131 INSTRUCTIONS
  FIXED AND FLOATING POINT ARITHMETIC
  SINGLE AND DOUBLE PRECISION ARITHMETIC
  INSTRUCTION WORD LENGTH — 16 AND 32 BITS
  DATA WORD LENGTH — 8/16/32 BITS
  VARIABLE LENGTH CHARACTER ADDRESSING
  MULTIPLE ACCUMULATORS
  MONITOR CLOCK
  MEMORY OVERLAP

• MEMORY
  TEMPERATURE STABLE COINCIDENT CURRENT CORE
  MODULAR IN UNITS OF 16,384 — 32 BIT WORDS
  EXPANDABLE TO 262,144 WORDS
  ASYNCHRONOUS OPERATION
  EIGHT ACCESSES PER MODULE
  1.5 MICROSECONDS CYCLE TIME
  BYTE SIZE 8/16/32 BITS
  INTERLEAVE

• INPUT/OUTPUT
  INDEPENDENT ASYNCHRONOUS PROGRAMMABLE
  I/O CONTROLLER
  EACH I/O CONTROLLER MAY COMMUNICATE WITH THREE CENTRAL
  PROCESSORS
  SIXTEEN CHANNELS PER I/O CONTROLLER
  OPTIONAL ELECTRICAL INTERFACES IN FOUR CHANNEL GROUPS
  NTDS SLOW (—15 VOLT)
  NTDS FAST (—3 VOLT)
  A-NEW (+3.5 VOLT)
  SERIAL
  INTEGRATED CIRCUIT BUFFER CONTROL MEMORY (64 WORDS)
  MAXIMUM INPUT/OUTPUT WORD RATE PER I/O CONTROLLER —
  167 KHZ (SINGLE-CHANNEL) NTDS FAST AND A-NEW, 41 KHZ
  (SINGLE CHANNEL) NTDS SLOW, 175 KHZ (SINGLE-CHANNEL)
  SERIAL, 1 MHZ (TOTAL INTERFACE)
  REAL TIME CLOCK

GENERAL CHARACTERISTICS

WHOLE-WORD, HALF-WORD OR QUARTER-WORD CAN BE
SELECTED FOR USE IN THE ARITHMETIC OPERAND
FULL DOUBLE-PRECISION FIXED POINT ARITHMETIC, INCLUDES ADD,
SUBTRACT, ENTER, STORE, TEST, AND BRANCH OPERATIONS
FLOATING POINT ARITHMETIC WITH MANTISSA LENGTH
OF 32 BITS AND A CHARACTERISTIC LENGTH OF 16 BITS
A SHIFT MATRIX ACCOMPLISHES MULTIPOSITION SHIFTS IN
ONE PLACE SHIFT TIME. SHIFTING CAN BE EITHER LOGICAL
(ZERO-FILLED), ARITHMETIC (SIGN-FILLED) OR CYCLIC
EIGHT ARITHMETIC ACCUMULATORS ALLOWS PARALLEL
AND CUMULATIVE COMPUTATION, DUPLICATE SETS OF
ACCUMULATORS FOR USE IN THE INTERRUPT AND TASK STATES
REGISTER-TO-REGISTER ARITHMETIC AND LOGICAL
OPERATIONS THROUGH THE USE OF HALF-WORD INSTRUCTIONS
A COMPLETE SET OF LOGICAL OPERATIONS AND
COMPARE INSTRUCTIONS

PHYSICAL

• CONSTRUCTION
  MODULAR, EXPANDABLE, CONDUCTION COOLING

• BASIC CONFIGURATION
  ONE CENTRAL PROCESSOR MODULE
  ONE INPUT/OUTPUT CONTROLLER MODULE
  ONE INPUT/OUTPUT ADAPTER MODULE (16 CHANNELS)
  THREE MEMORY MODULES (49,152 WORDS)
  ONE POWER SUPPLY MODULE
  ONE MAINTENANCE CONSOLE

• VOLUME (BASIC)
  10.4 CUBIC FEET

• WEIGHT (BASIC)
  500 POUNDS

• POWER CONSUMPTION
  2300 WATTS (BASIC SYSTEM)

• SIZE
  41 IN. HEIGHT, 20 IN. WIDTH, 22 IN. DEPTH

• MAINTENANCE
  THROW AWAY PRINTED CIRCUIT CARDS

• RELIABILITY
  2000 HOURS MTBF (EST.)

• ENVIRONMENTAL
  MIL-E-16400 CLASS 1

• OPERATING TEMPERATURE
  −54°C TO +65°C

• NON-OPERATING TEMPERATURE
  −62°C TO +75°C

• VIBRATION
  MIL-STD-167, TYPE 1

• SHOCK
  MIL-S-901, CLASS 1, GRADE A
FAST...COMPACT...RELIABLE

AN/UYK-7(V) is designed to perform data processing tasks in a more reliable, real-time manner, and with greater speed and efficiency, than ever before.

Using creative hardware design, Univac has developed the AN/UYK-7(V) into a highly flexible computing system. The system can perform all data processing tasks now handled by a series of unit computers. The use of modular design permits a new level of equipment standardization. Standard modules simplify logistic and support requirements, and greatly reduce over-all user costs.

Support software and a powerful instruction repertoire provide the facility for developing and debugging computer programs.

Fast, compact and reliable, the AN/UYK-7(V) is ready to carry out a diversity of shipboard data processing tasks — now and in the future.

FEDERAL SYSTEMS DIVISION

Univac Federal Systems Division has for many years devoted a major portion of its resources to the solution of real-time military problems encountered in weapons control, command and decision, and instrumentation systems. This experience has encompassed all types of military environments including airborne, spaceborne, shipboard, ground mobile and fixed sites. Because of its concentration in these areas, Univac has developed the unique scientific research, engineering design and development, and the organizational structures necessary for designing, developing and manufacturing "state-of-the-art" digital computing systems.

In addition, as a Division of the Sperry Rand Corporation, Univac has available, through the diversified resources of other corporate divisions, the synergistic scope of capabilities and disciplines required by today's complex systems problems.
REGIONAL OFFICES

1325 No. Atlantic Avenue
Holiday Office Center
Cocoa Beach, Florida 32931
(305) 784-1545
403 Braniff Towers
Exchange Park
Dallas, Texas 75235
(214) 358-1583/84/85
5160 Springfield Street
Dayton, Ohio 45431
(613) 253-8157
8888 Dyer Street
El Paso, Texas 79904
(915) 751-6435
3322 So. Memorial Parkway
Suite 22
Huntsville, Alabama 35802
(205) 881-9105/9100
6151 West Century Blvd.
Suite 203
Los Angeles, California 90045
(213) 776-6171
260 Sheridan Avenue
Suite 403
Palo Alto, California 94306
(415) 327-6880
322 North 21st West
Salt Lake City, Utah 84116
(801) 328-8066
808 East Mill Street
Suite 219
San Bernardino, California 92410
(714) 889-1096
3045 Rosecrans Avenue
Gross Center
San Diego, California 92106
(714) 224-3693/4
400 Totten Pond Road
Bear Hill Industrial Park
Waltham, Massachusetts 02154
(617) 899-4110
2121 Wisconsin Avenue, N.W.
Washington, D.C. 20007
(202) 338-8500
3500 Virginia Beach Blvd.
Malibu Towers, Suite 505
Virginia Beach, Virginia
(703) 486-3111

Additional information for the AN/UYK-7(V) system application may be obtained from the regional offices or:

Univac Federal Systems Division
Director, Navy Marketing
Univac Park
Box 3525
St. Paul, Minnesota 55101
(612) 456-2222
Thank you for your interest in UNIVAC–Division of Sperry Rand Corporation and, in particular, our newly announced AN/UYK-7 Military Computer System. In response to your recent request, we have enclosed a brief descriptive brochure covering this equipment.

If, after reviewing this data, you should wish additional information for your application, please call our representative in your area as listed below or contact me directly in St. Paul.

Thank you for this opportunity to be of service.

Sincerely,

UNIVAC–Division of Sperry Rand
Federal Systems Division

L. J. Franklin
Sales Manager–Command and Information Systems Marketing

612/456-2406

Louis Dentino
260 Sheraton Avenue
Palo Alto
California 94308

LJF/amw
Enclosure