An IT Legacy Paper for November ‘17

- History of the ERA formation and ensuing Corporate names – excludes the defense systems path to LMCO
- 1100/2200 Evolution
- Technology history of the systems
- The evolution of the computer circuit technologies.
- Slide Credit to R. Angvall via Ron Q. Smith

History

Stuff Happens

B.C.
30,000-17,000
Paintings of animals made in caves by Stone Age artists

3000-2050
Ur of the Chaldeans; occupied before 3000

2650-2500
Pyramids of Gizeh, near Cairo, erected

1900-1700
Stonehenge, Salisbury Plain, England; Stone Age circle of stones

1800
Babylonian King Hammurabi's code of laws set in stone

1450
Mycenaeans wrote in Linear Script B on clay tablets

1200
Fall of Troy

705-681
Sennacherib built up Nineveh

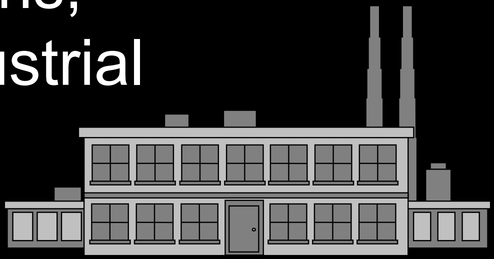
500-400
Athen's Golden Age

100
First of Dead Sea Scrolls - Biblical manuscripts - written

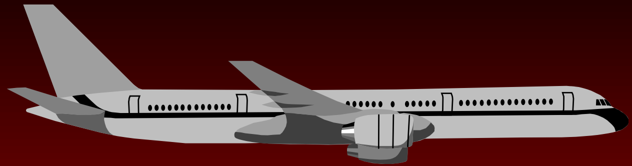
A.D.
650-670
Burial of Saxon ship and treasure at Sutton Hoo

Some Time Later...

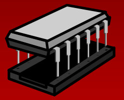
- A few centuries, wars, famines, kings, queens, caesars, czars and presidents later the industrial revolution began to change our lives



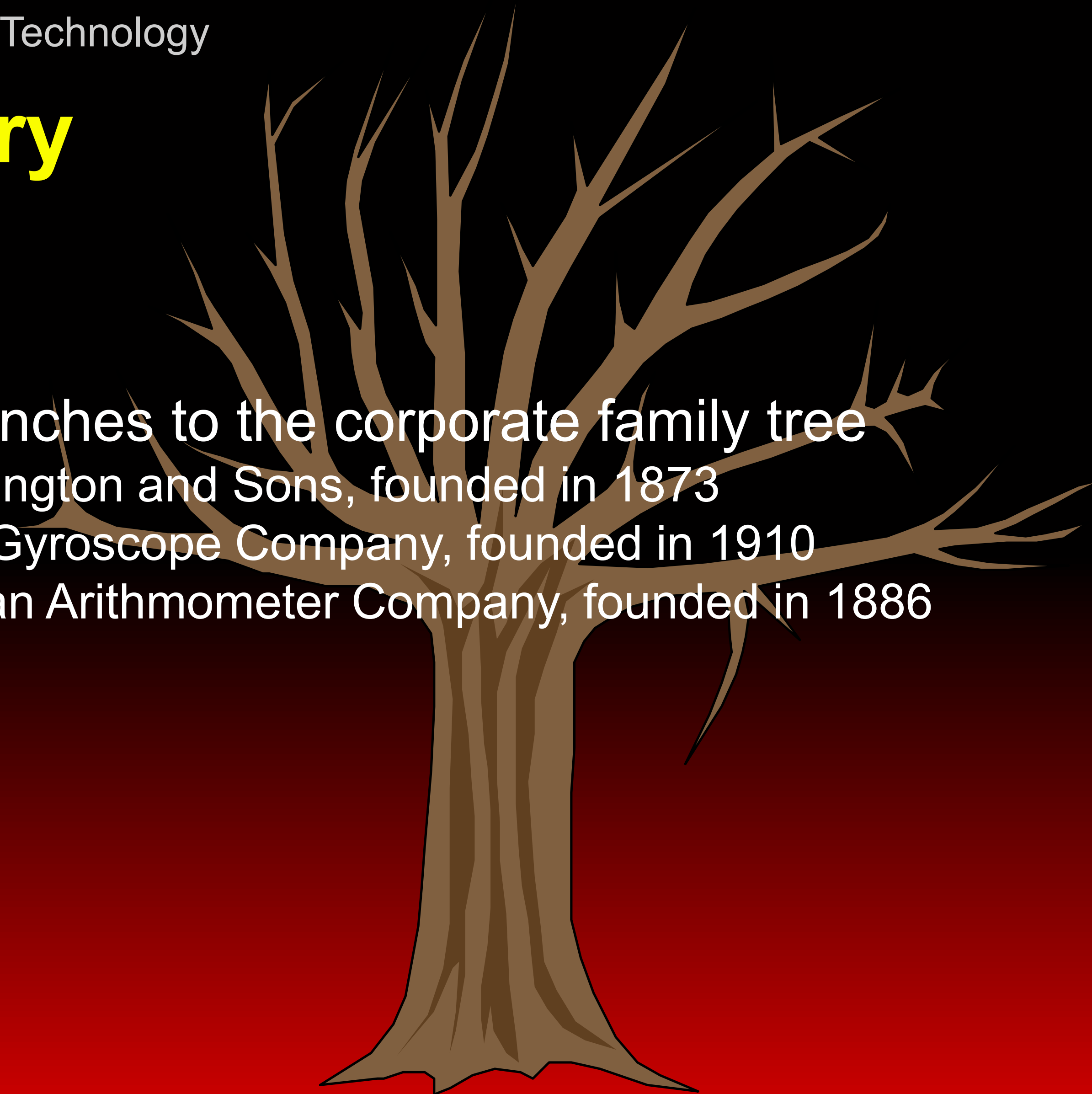
- Bicycles, automobiles, trains and airplanes began to change our lives even more



- A device or system that is capable of carrying out a sequence of operations in a distinctly and explicitly defined manner was created to change our lives in ways never imagined



History



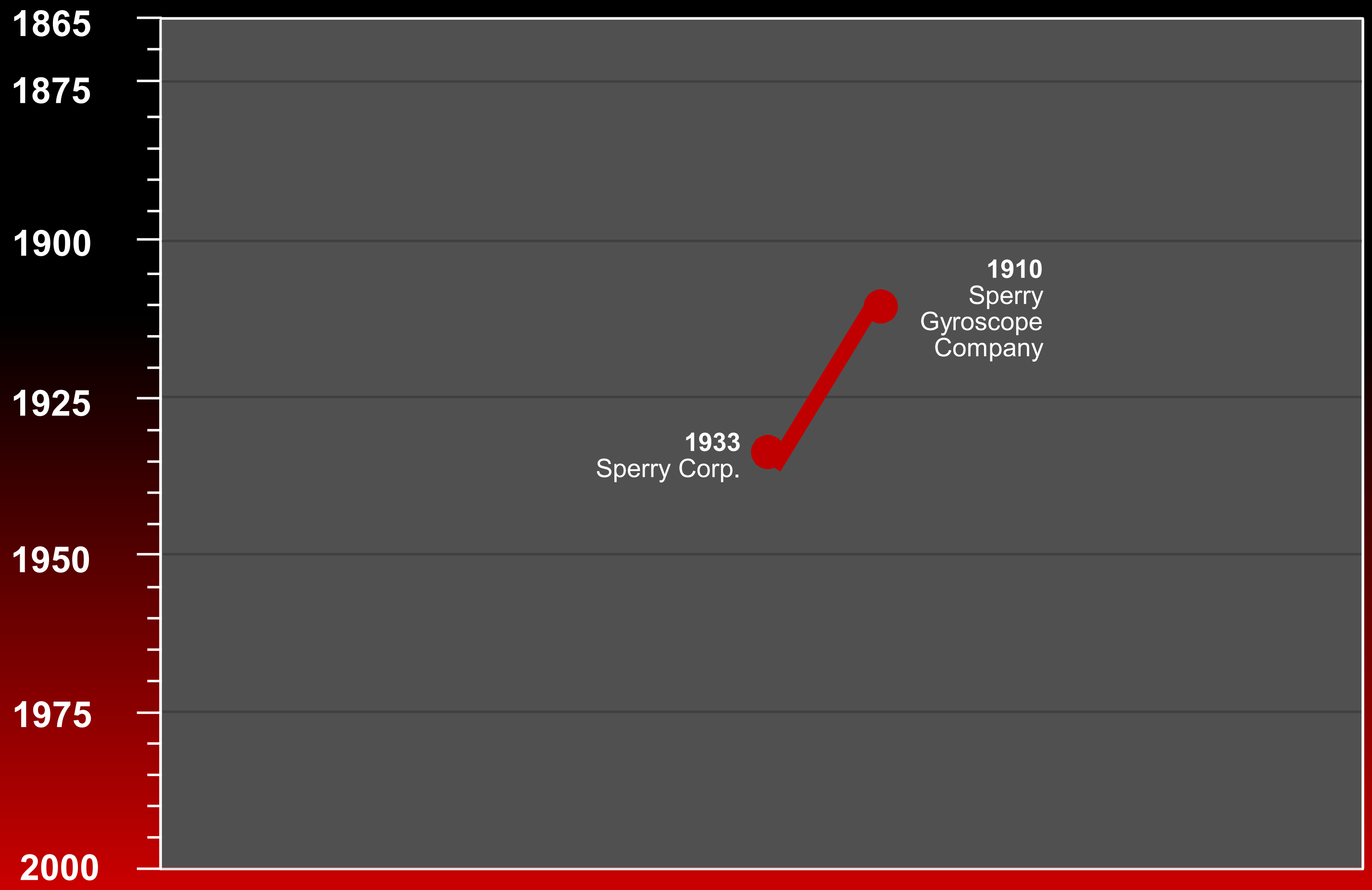
- Tree branches to the corporate family tree
  - –E. Remington and Sons, founded in 1873
  - –Sperry Gyroscope Company, founded in 1910
  - –American Arithmometer Company, founded in 1886

The E. Remington Branch

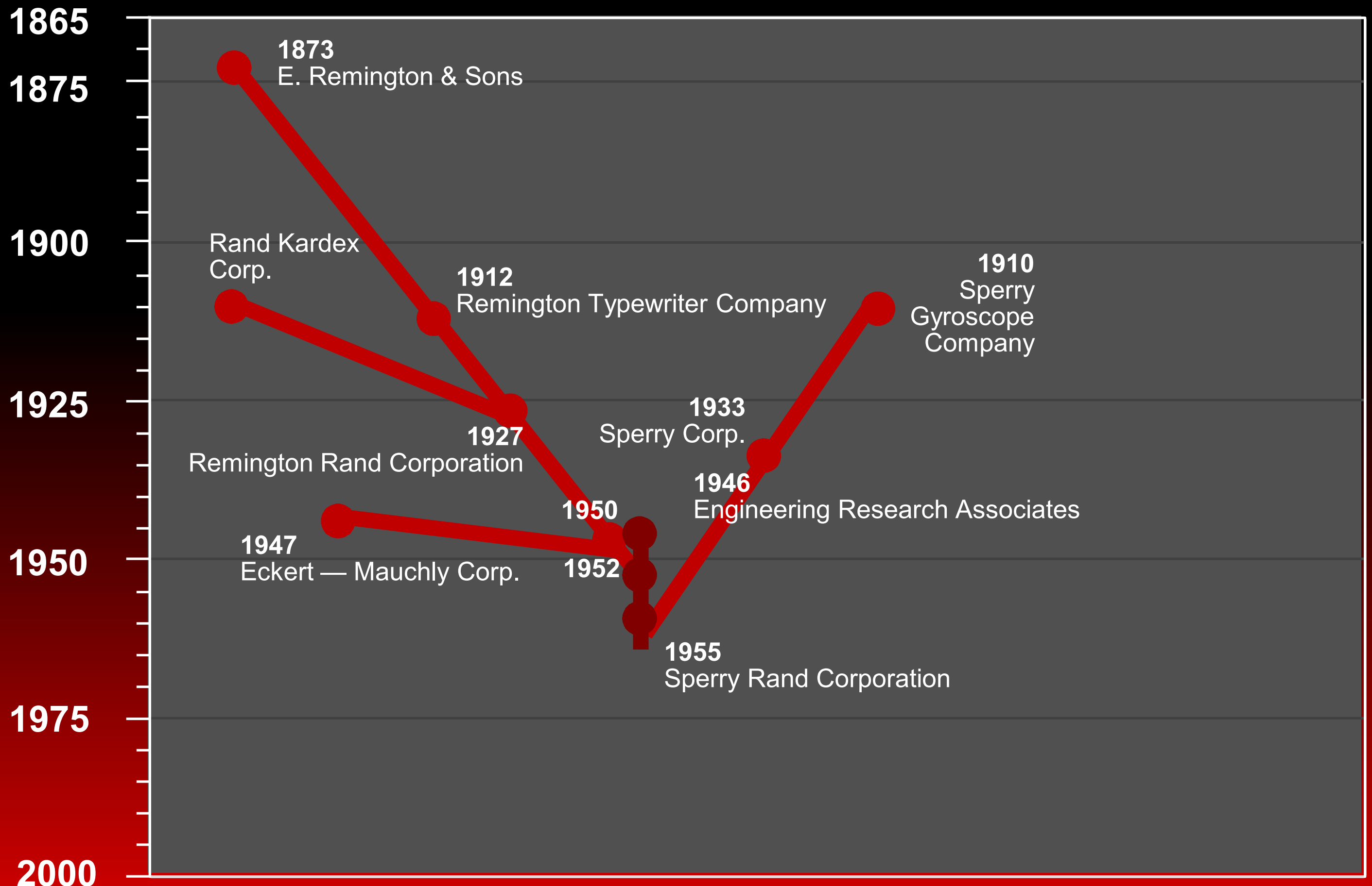
The Entrance of Eckert-Mauchly Corporation

The Entrance of ERA

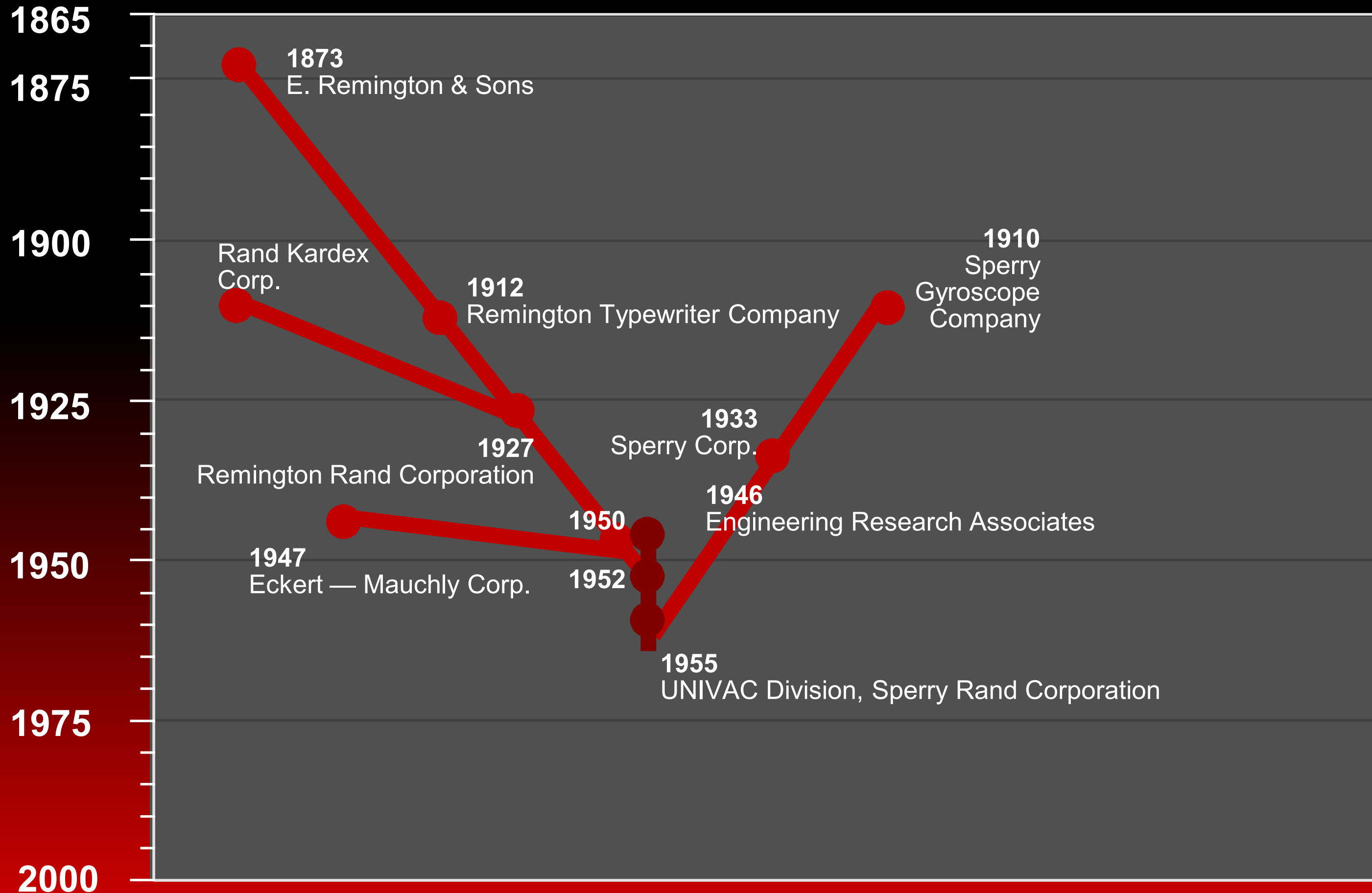
The Sperry Gyroscope Branch



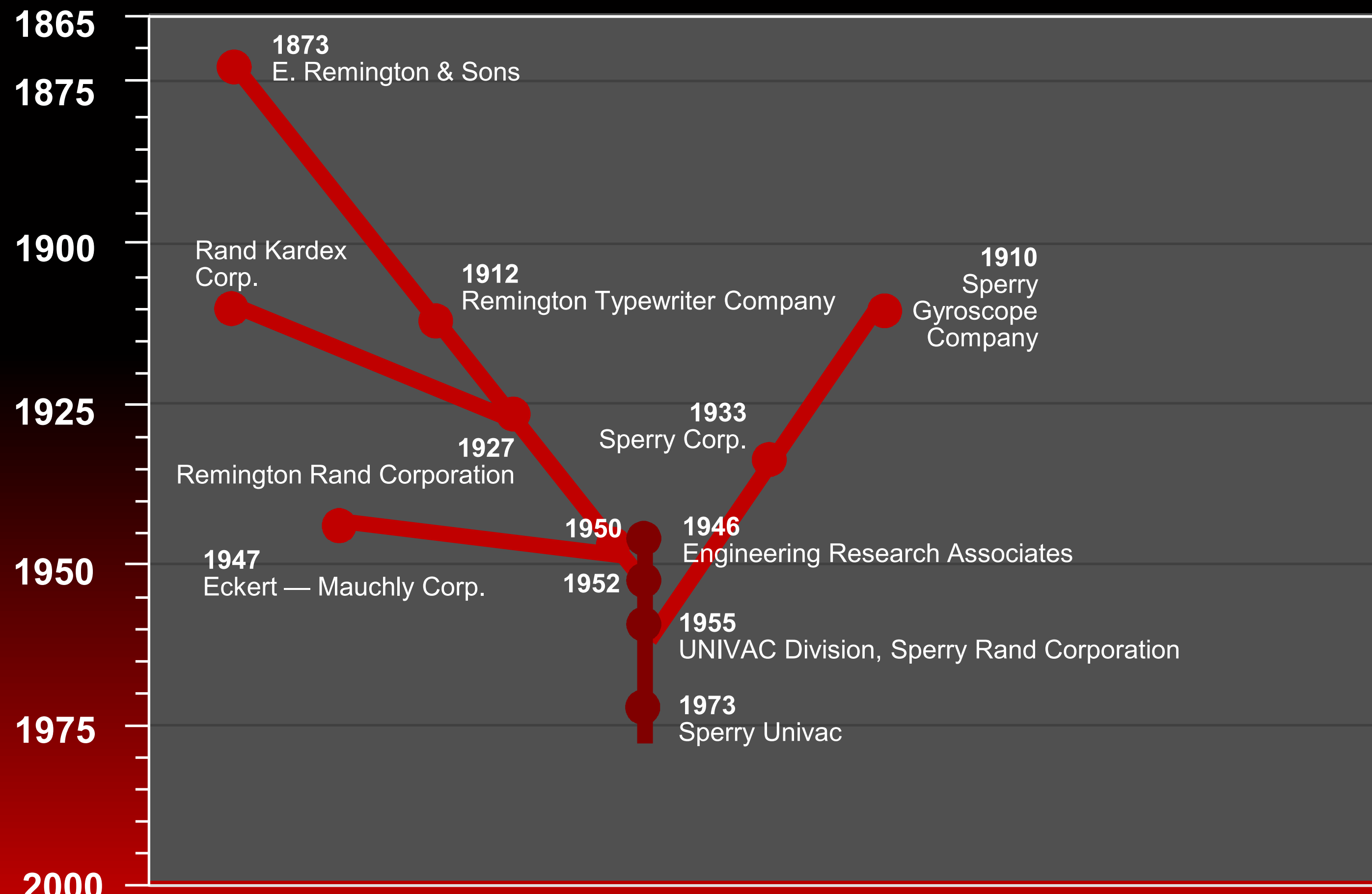
The Formation of Sperry Rand Corporation



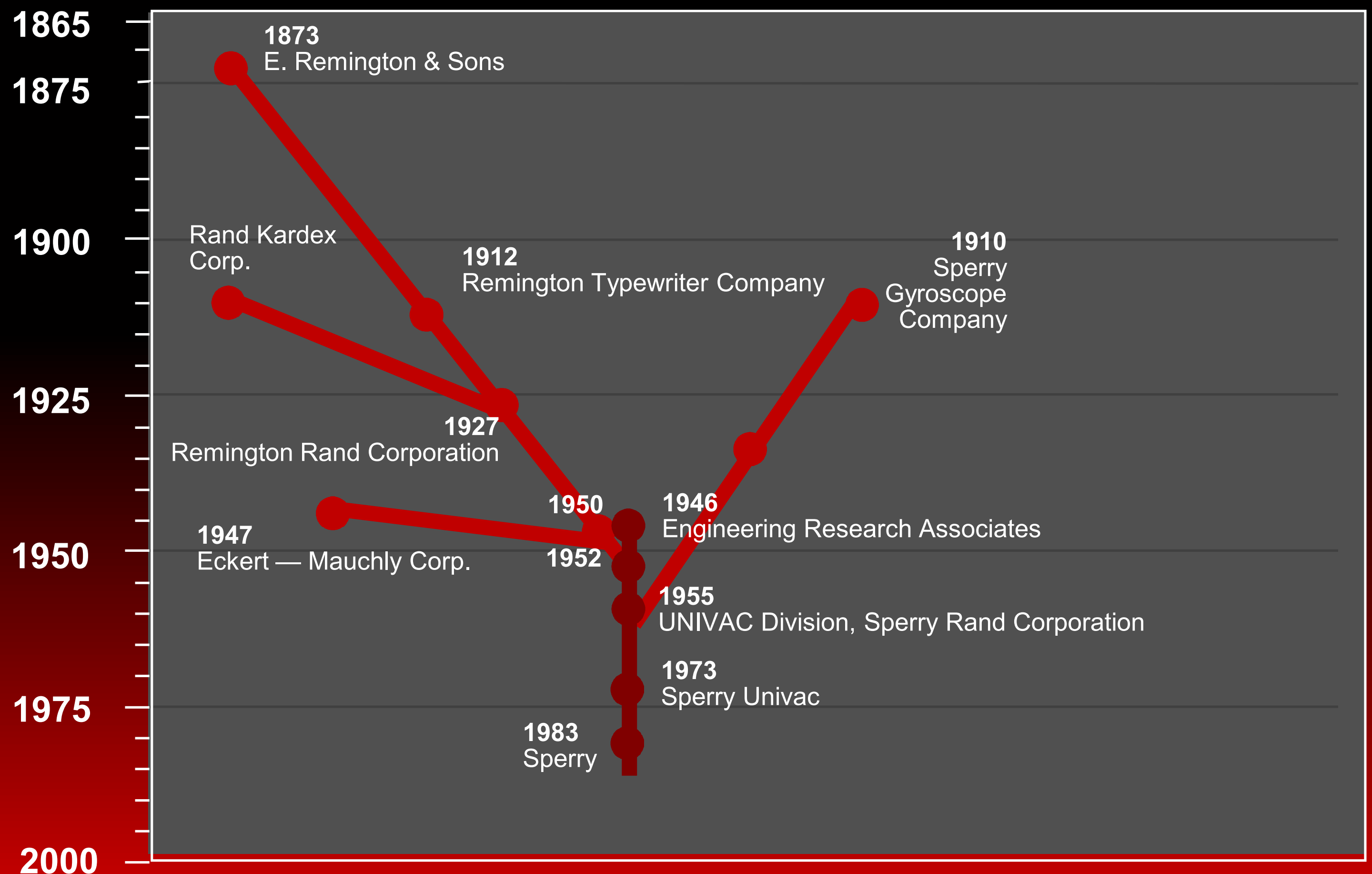
The Formation of Univac



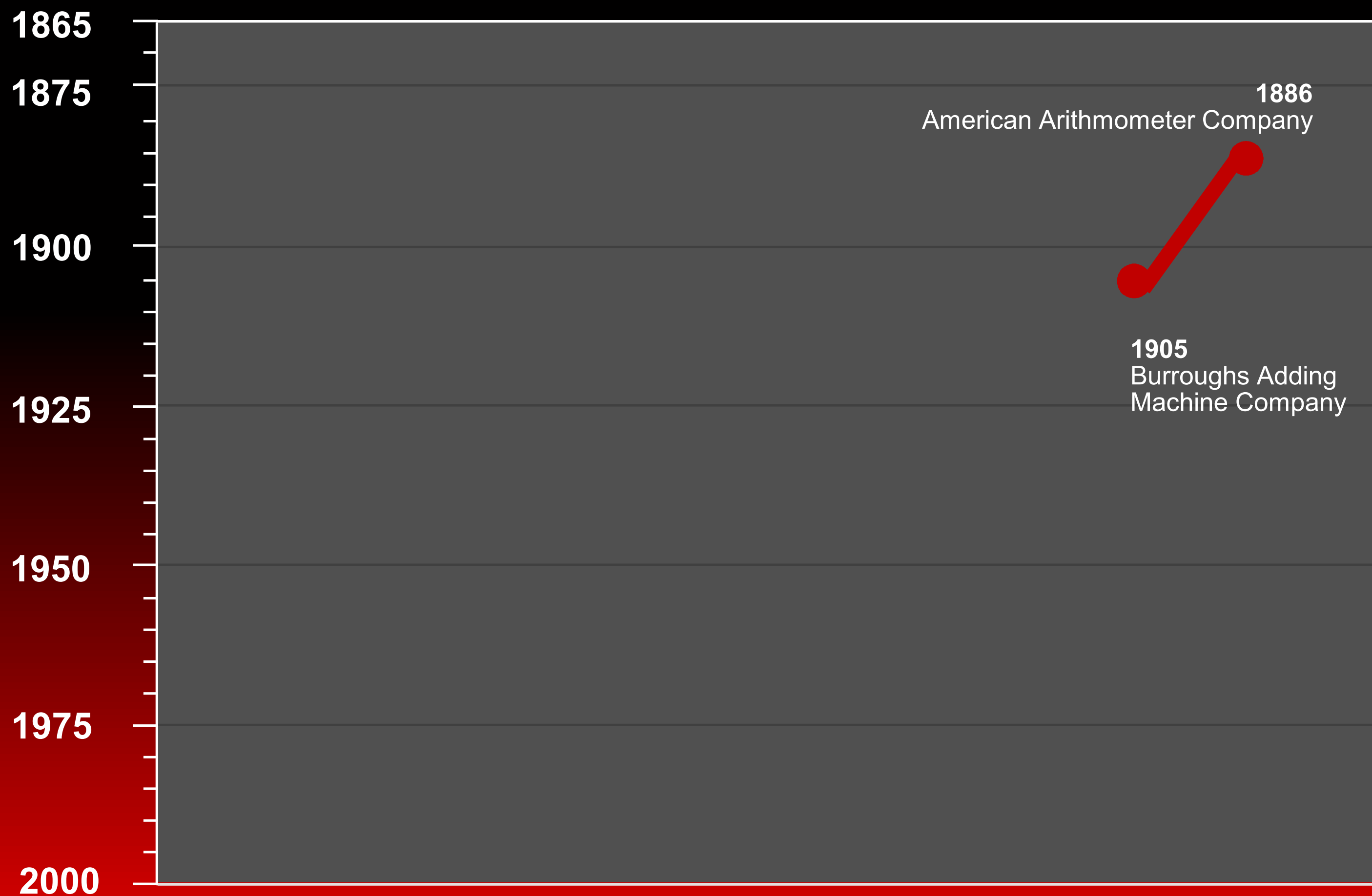
The Name Change to Sperry Univac



The Name Change to Sperry Corp.

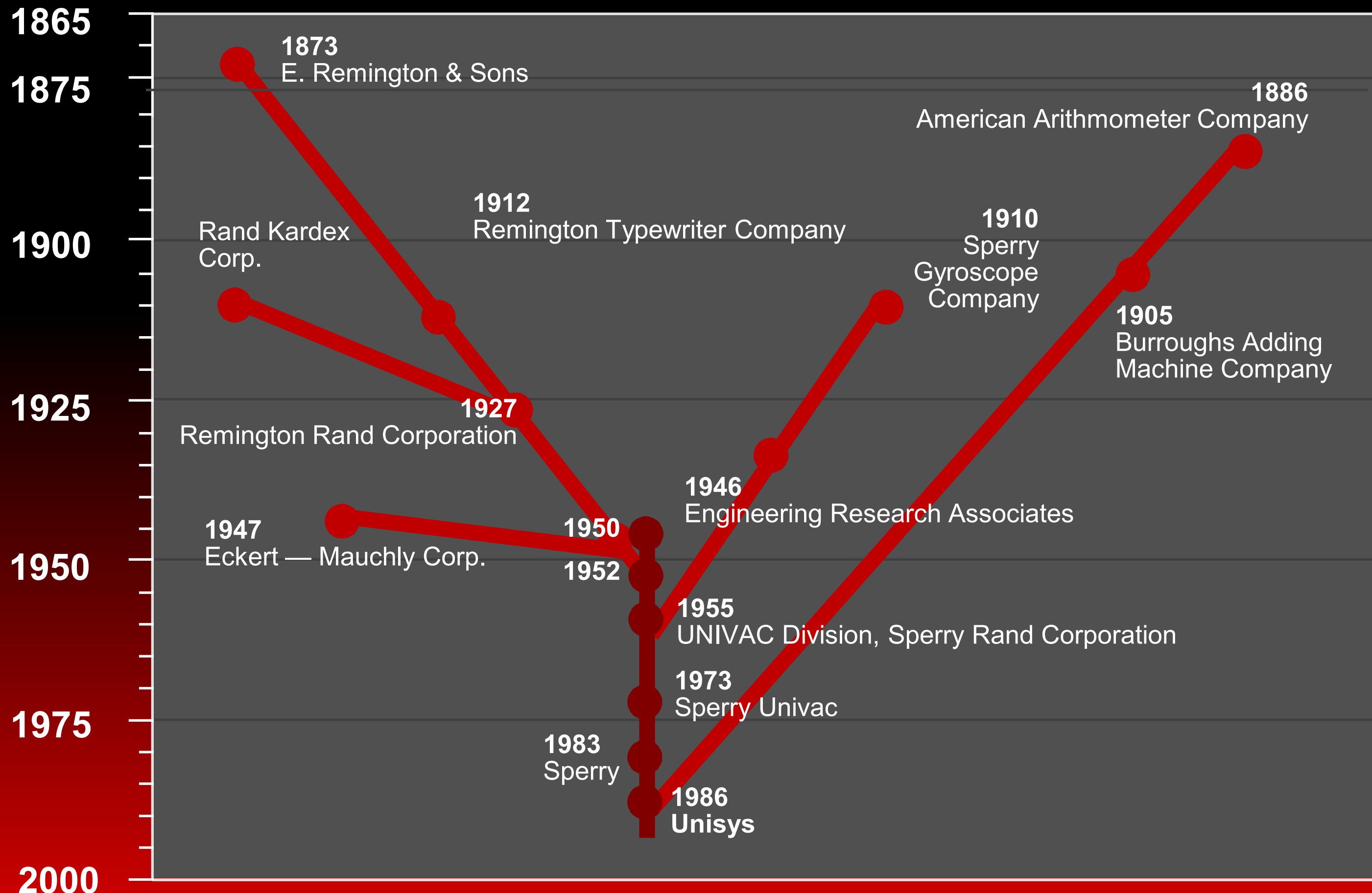


The American Arithmometer Branch



History and Technology

The Formation of Unisys



1100/2200 Evolution

Unisys

SPERRY

Sperry Univac

Sperry Rand

Remington Rand

ERA

1950	1960	1970	1980	1990
1103 1101	1108 1107	1100/60 1100/80 1110	2200/400 2200/600 2200/200 System 11 1100/90	XPC 2200/500 2200/900

1100 System Timeline

1947	ERA starts work on Task 13
1950	Atlas I delivered to Navy
1951	1101 24 bits, 16K, drum memory
1953	1103 36 bits, 8K, core memory
1957	1105 faster, 12K, core memory
1961	1107 65K thin film registers, two banks
1965	1108 131K core memory, guard mode
1968	1108A 262K memory, multiprocessing
1969	1106 slowed down 1108A
1972	1110 262K plated wire, 1M extended storage, 6 processors
1975	1100/20, 1100/40 semiconductor memory
1977	1100/80 4M memory, cache
1979	1100/60 extended instruction set
1981	1100/70 1 cabinet 1100/60

1100 System Timeline

C-Series Architecture

1984	1100/90, System-11 extended mode, 16 M memory
1987	2200/200 VLSI 1100 chip set
1988	2200/600 new IP and memory for 1100/90
1989	2200/400 common I/O system

1100 System Timeline
M-Series Architecture

1990	2200/100 smaller/200, 2200/600ES new IO
1992	2200/900 paging, 1GW memory, 8 IPs
1993	2200/900E entry level 2200/900, 2200/500 mid-level, rack mount, 2200/900 commonality XPC data acceleration
1994	2200/500E, 2200/500SE, 2200/500M and 2200/500ME extensions of 2200/500 product range
1995	2200/300 entry level system, 2200/700 high mid-range

Technology

1940s ERA
Atlas I

- U.S. Navy Task 13 started August,
  - 1947 delivered in 1950
- CPU
  - 24-bit word
  - 5 microsecond integer add + memory access

1940s ERA
Atlas I , (cont'd)

- Memory
  - –16K word magnetic drum
  - –32 - 17,000 microsecond access time
- Technology
  - –2,695 vacuum tubes (18 types)
  - –2,385 diodes

1950s
1101

- Commercial version of Atlas I
- First “1100”
- Task 13 = 1101 binary
- 24 bit word
- Vacuum tube amplifiers

1950s
1101

- Crystal diode logic
- Magnetic drum memory
- Input - paper tape
- Output - paper tape and typewriter

1950s
1103

- 36 bit word
- First commercial use of “1100”
- 3,900 tubes, 5,000 diodes
- 16K word drum memory
- 1K word electrostatic storage tube - first five units

1950s
1103

- 1K core memory - next four units
- 4K core memory (1103A)
  - 420 tubes, 2,2000 diodes
  - 12 microsecond cycle time

1960s
1107

- Transistor/diode logic
- 80 nanosecond logic gate
- Wire wrap backpanel
- 65K word core memory
  - –4 microsecond cycle
- Magnetic film memory - 128 words
  - –Original General Register Set (GRS)
  - –0.6 microsecond cycle

1960s
1108

- High-end system
- Multiprocessor organization
- Improved transistor/diode logic circuit
- 15 nanocsecond logic gate
- Four to five times 1107 performance

1960s
1108

- One bit integrated circuit chip
  - Replaced magnetic film memory
  - 0.125 microsecond cycle time
- 64K word core memory cabinet
  - 0.75 microsecond cycle time
- 256K word maximum on system

1960s
1106

- Mid-level system
- Slower version processor of 1108
- Cost reduced 1.5 microsecond core memory

1970s
1110

- 1108 follow-on
- Integrated circuit logic
- 10 nanosecond gate switching delay
- 12 or 14 integrated circuit board layers
- Two level memory

1970s
1110

- Cost reduced core memory
- Plated wire memory
  - –300 nanosecond read cycle
- Separate I/O cabinet

1970s
1100/40

- Upgraded 1110 system
- Metal Oxide Semiconductor (MOS) memory replaces core and plated wire memory

1970s
1100/80

- 1110 follow-on
- Emitter Coupled Logic (ECL)
  - –3 nanosecond logic gate
- Precision multilayer printed circuit cards
- Multilayer backpanels

1970s
1100/80

- Cache memory organization
- All semiconductor memory
  - –4K: 16K bit chips
- Two million words per cabinet

1970s
1100/60 and 1100/70

- 1106 follow-on
- Multimicroproccessor CPU
- Microprogrammed logic
- 12 or 14 integrated circuit board layers

1970s
1110/60 and 1100/70

- Single cabinet
  - –CPU, memory, I/O
- Greatly expanded 1100 user base
- Several generations of memory chips

1980s
1100/90

- 1100/80 follow-on
- 3.5 times performance of 1100/80
- LSI logic
- 390 picosecond gate switching delay
- 300 gates per chip
- 6000 chips per processor

1980s
1100/90

- 19 or 22 integrated circuit board layers
- 52 integrated circuit boards per processor and cache
- 64K memory chips
- 96 I/O channels

1980s
1100/90

- Instruction processor, memory and I/O built in accordance with the C-Series architecture
- Introduced “Extended Mode” processing
- Foundation for the “New Programming Environment”

1980s
2200/200

- Low-end systems
- CMOS - VLSI chip set
  - Six chip, 1100 CPU
  - 30,000 gates per chip
- One card processor
- 256K memory chip
- Bus and I/O modules carried over from System 11

1980s
2200/600

- 1100/90 follow-on
- 2+ times performance of 1100/90
- VLSI logic
- 200 picosecond gate switching delay
- 2000 gates per chip

1980s
2200/600

- 24 integrated circuit board layers
- 18 integrated circuit boards per processor and cache
- 1 megabit memory chips (4-16MW/cabinet)
- 96 I/O channels

1980s
2200/400

- 1100/60-70 follow-on
- 2 to 3 times performance of 1100/60
- VLSI CMOS logic
- 5 nanosecond gate switching delay
- 125,000 gates per chip
- 2381 chips per processor

1980s
2200/400

- 12 integrated circuit board layers
- 1 integrated circuit board per processor and cache
- 1 megabit memory chips
  - (16MW max - 4MW/board)
- New CMOS VLSI I/O section

1990s
2200/100

- New compact, low end system
- Extension of 2200/200
- Integrated peripherals

1990s
2200/600ES

- Extension of 2200/600
- Single cabinet CPU and memory
- CMOS VLSI I/O modules
- Less space, less power consumption

1990s
2200/900

- 2200/600 follow-on
- 2 times performance of 2200/600
- VLSI logic
- Multi chip RAM/gate array logic
- 100 picosecond gate switching delay
- 9000 gates per chip

1990s
2200/900

- 197 chips per processor
- 50 integrated circuit board layers
- 1 integrated circuit board per processor and cache
- 1 megabit memory chips
  - (64MW-128MW/cabinet)
- 384 I/O channels

1990s
2200/900

- Increased processing capacity with up to 8 instruction processors
- New second level cache (SLC)
- Dramatic increase in memory size - up to 512MW
- New System Control Facility
- Extended Processing Architecture providing enabling technologies for extension and growth

1990s
2200/900

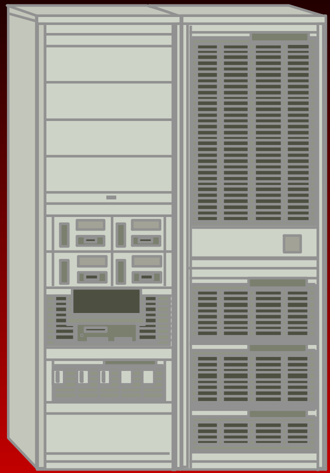
- Instruction processor, memory and I/O built in accordance with the M-Series component of the Extended Processing Architecture
- Extends capabilities of “Extended Mode” processing
- Provision of expanded physical memory and virtually unlimited logical memory provides new paradigm for progamming

1990s
2200/900E

- Speed reduced 2200/900
- Limited models
- Field upgradable to 2200/900

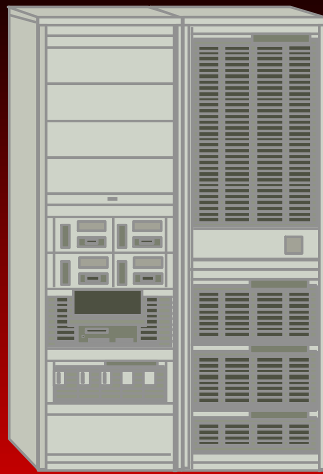
1990s
2200/500

- Low-end and mid-level system
- 2 1/2 to 3 times performance of 2200/400
- VLSI logic
- 500 picosecond gate switching delay
- 300,000 gates per chip, ca.100,000 used
- 18 chips per processor



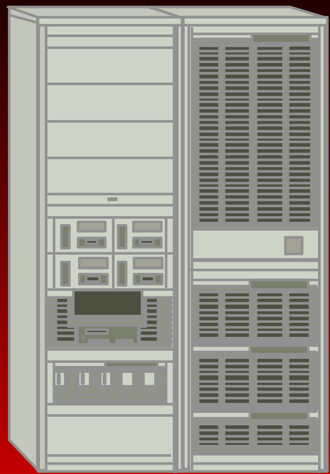
1990s
2200/500

- 22 board layers
- 1 integrated circuit board per processor and cache
- 1 megabit memory chips
  - (32-128MW/cabinet)
- 128 I/O channels (4 cabinets)



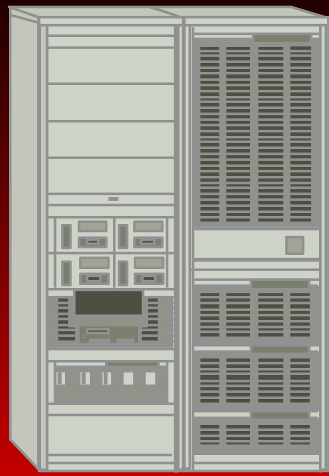
1990s
2200/500

- 2200/900 commonality
  - –IP/SC design translated to CMOS
  - –SCSI and BMC channels
  - –System control
  - –Software
- The second XPA based system
  - –Successor to C Series
  - –Based on M-Series



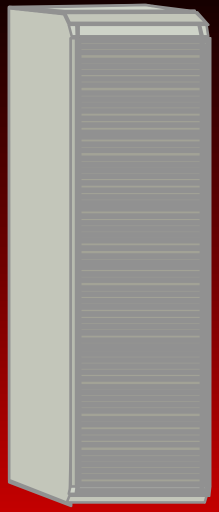
1990s
2200/500

- Many model ranges:
  - –Entry
    - -2200/500SE
    - -2200/500E
    - -2200/500ME
  - –Midrange
    - -2200/500 1x - 4x
    - -2200/500M
  - –Upper Midrange
  - –2200/500 5x - 8x
- UC36 Unisys common packaging
- 19” rack mountable components



1990s
Extended Processing Complex

- An intelligent memory-based CEC component that connects to one or more hosts
- Accelerates I/O transfers
- Provides multi-host file-locking and communication
- Improves resource management



1990s
Extended Processing Complex

- Many new components
  - –Host based Data Mover (DM)
  - –XPC based Host Interface Adapter (HIA)
  - –Light pipes connecting DMs to HIAs . . .
- Multiple models, with optional memory sizes

Advances in 2200 Series Processor Technology

	1100/90	2200/600	2200/900	2200/500
Year of Intoduction	1984	1989	1992	1993
Gates/Chip	300	2,000	9,000	300,000 ca. 100K used
Gate Switching Delay	390 nsec	200 psec	100 psec	500 psec
Gates per Processor	600,000	630,000	824,000	731,000
Chips per Processor	6,000	850	196	18
Boards per Processor	52	18	1	1

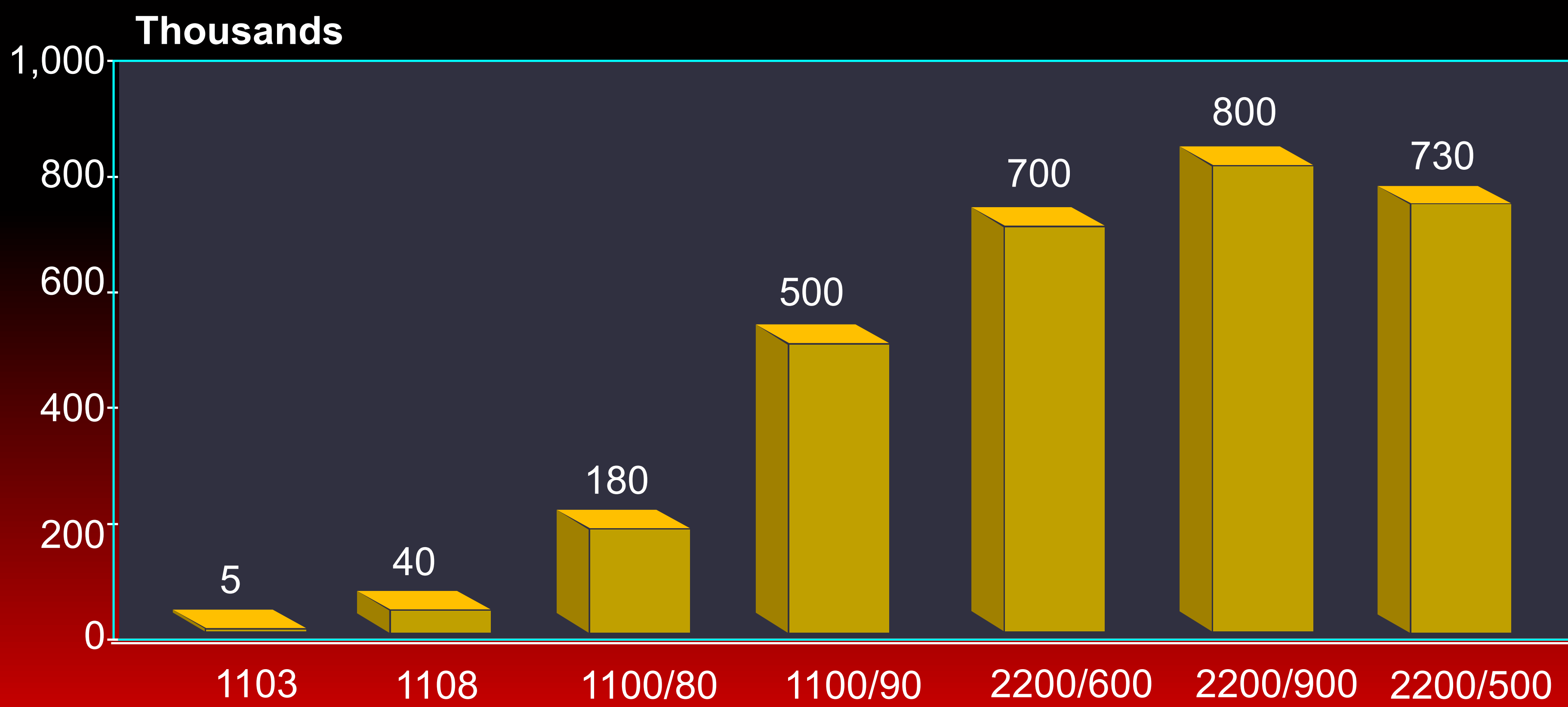
Technology Trends

Technology Trends

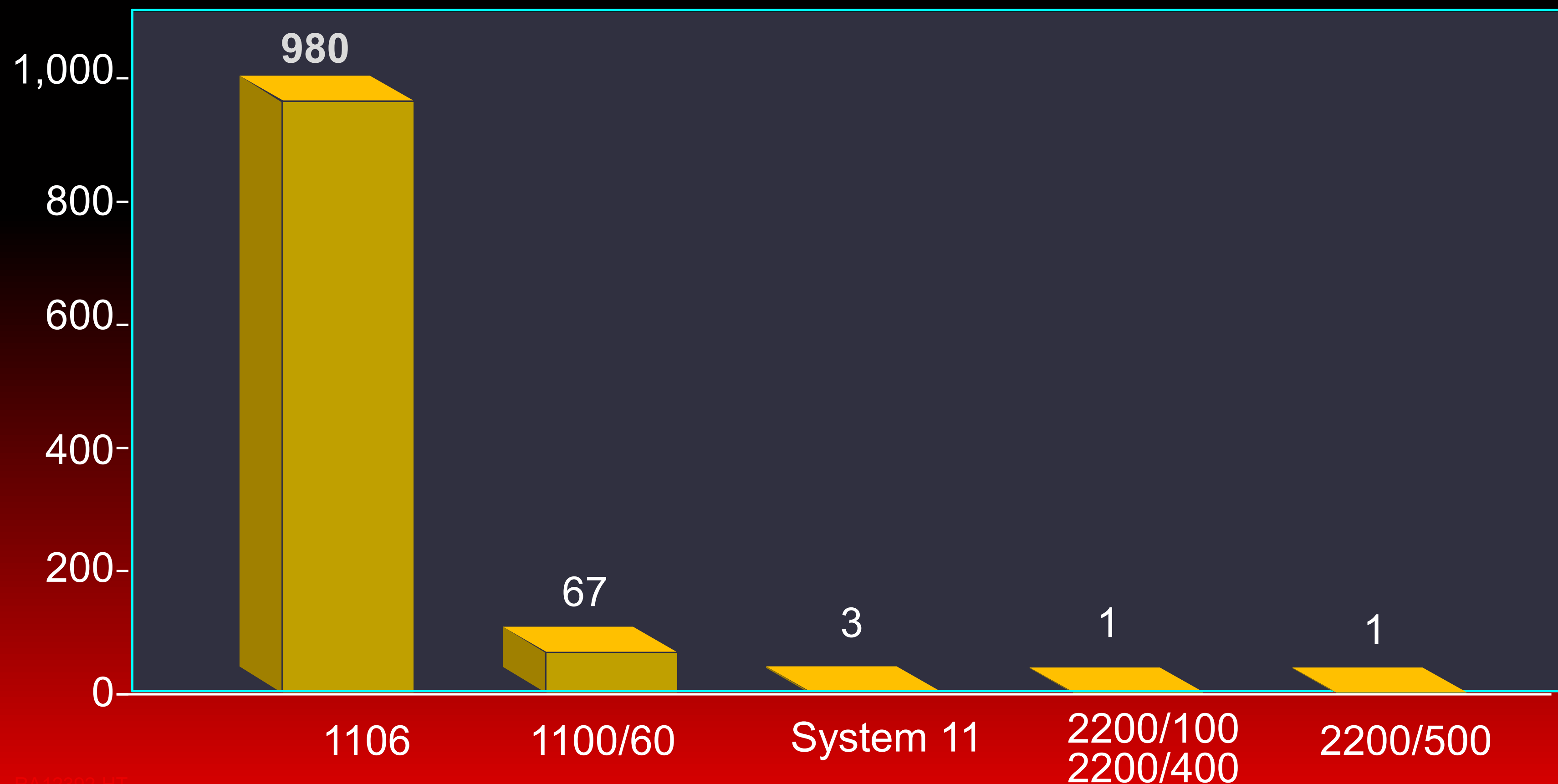
Technology trends have developed from generation to generation

- –Increase in logic density per chip
- –Decrease in basic gate switching delay
- –Decrease in chips per processor
- –Increase in layers per IC board
- –Decrease in IC boards per processor
- –Increase in processors
- –Increase in I/O connectivity

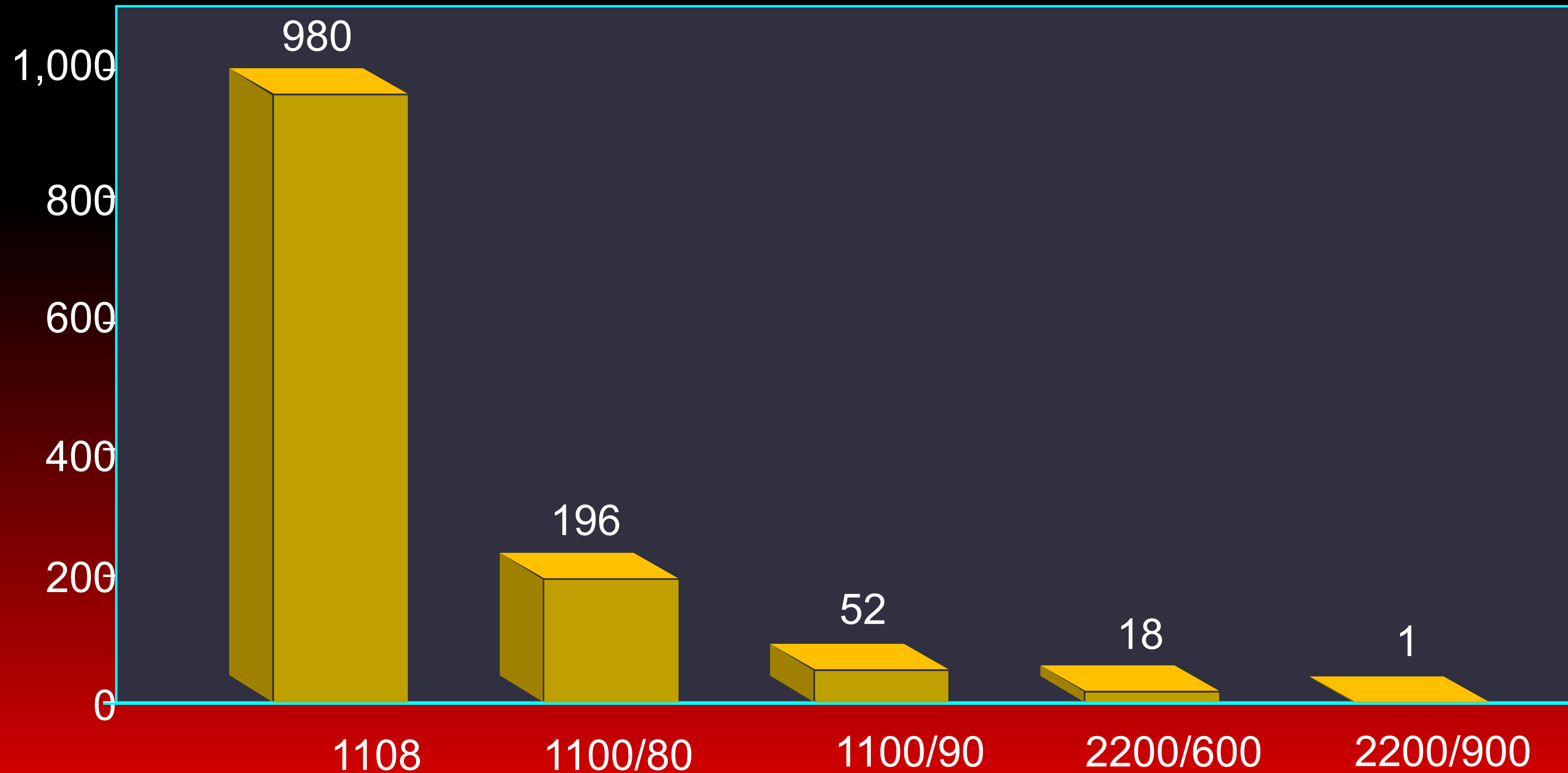
Processor Logic Gates



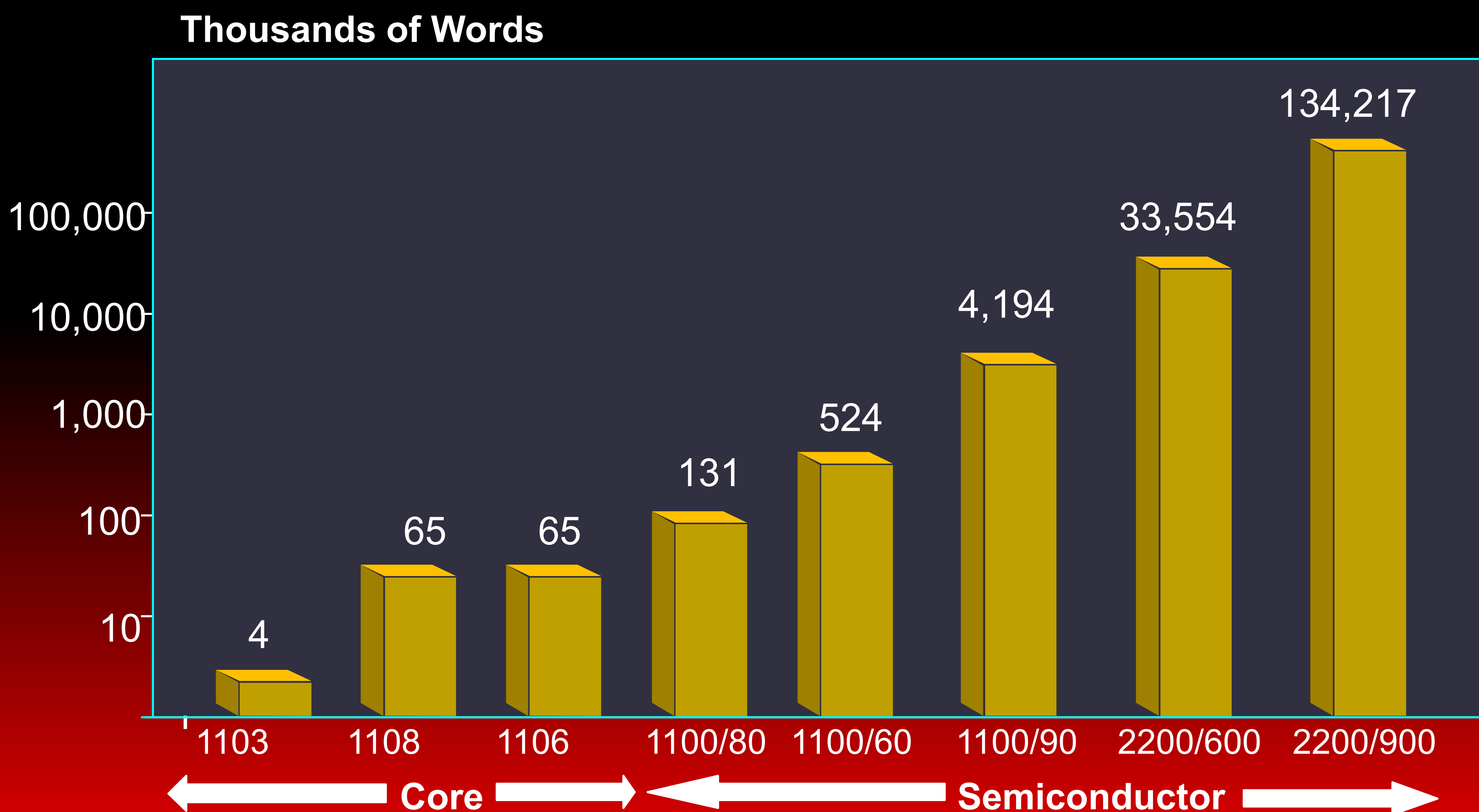
Processor Printed Circuit Cards
Low - Medium Performance Systems



Processor Printed Circuit Cards
High Performance Systems



Memory Capacity per Cabinet



UNISYS