VIP CLUB
Established in 1980

Micro-1100 Story

Introduction

The Micro-1100 CPU Chip Set Development project started in January 1983 when Carl Johnson was invited to a meeting with managers from Sperry's Roseville Engineering, Semiconductor Operations, Roseville Controller Office, and Facility Management. They offered him support to assemble logic designers, silicon designers, and CAD design experts along with a secure Roseville space and a planning/procurement budget reporting to the VP of Engineering. That was the beginning of Micro Product Development, which peaked at some 24 employees under Sperry Director Carl Johnson.

Carl provided the data for this paper from his personal archives. Researchers may also see some of the original development description papers in the archives at the Charles Babbage Institute, University of MN; http://vipclubmn.org/Articles/CarlJohnsonPapers.pdf.

Sperry Management had developed many shadowboxes to exhibit their technologies, now at the UNISYS Eagan facility, http://vipclubmn.org/Articles/ThroughTheAges.pdf. As a complement to those displays, Carl has now created and donated two wall mount display boards – exhibited at the Lawshe Memorial Museum in S. St. Paul along with other artifacts from the Legacy committee.

This paper has an early press article, two Micro-1100 display board photos, related excerpts from previous 'Our Stories', Mr. Johnson's 1985 presentation slides, and micro biographies.

From the Press

"Sperry puts mainframe on five CMOS chips! Electronics/ April 19, 1984

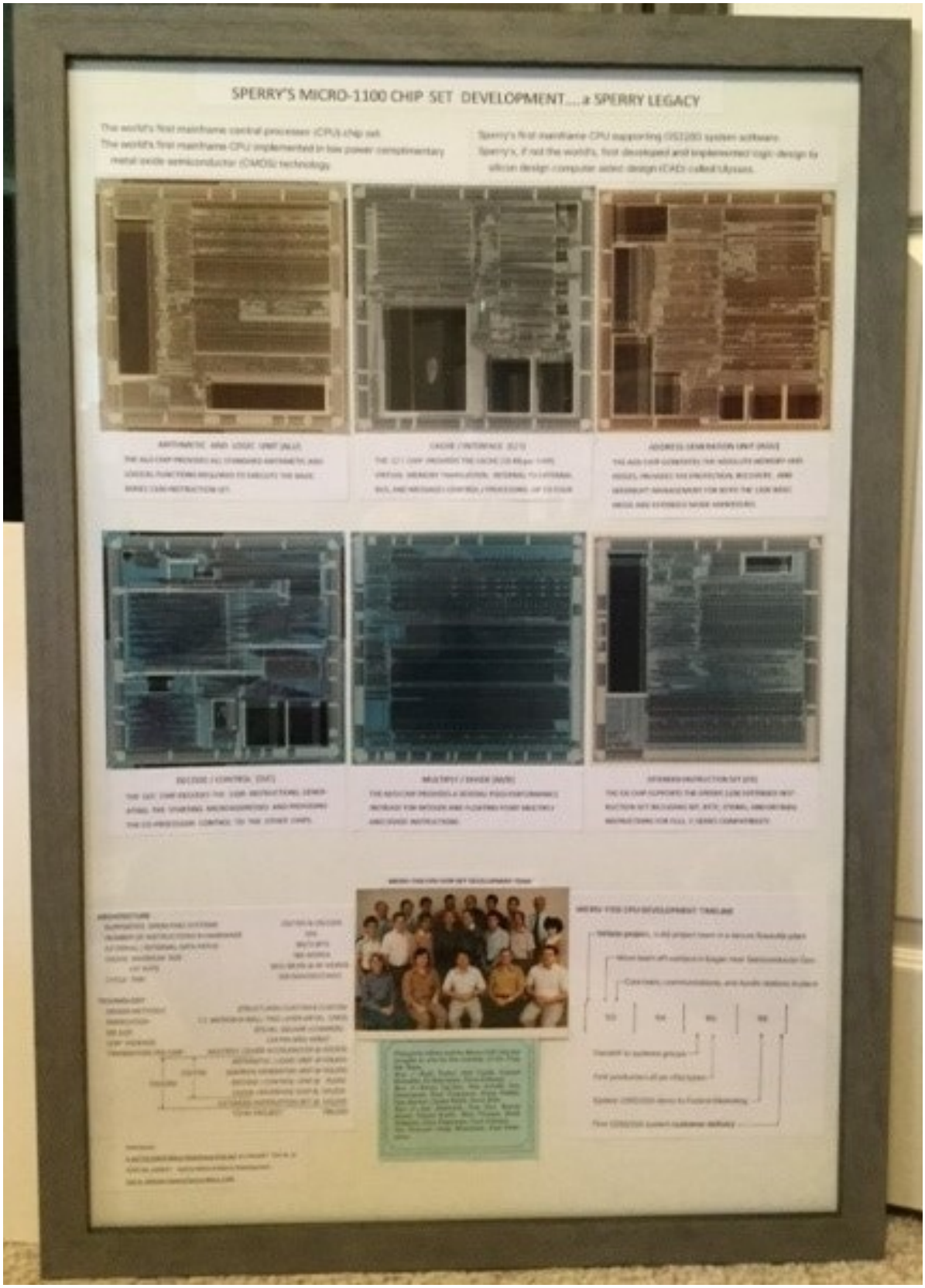
The (World's) first mainframe-class CPU Chip Set development, Sperry's Micro-1100 CPU, was recognized and reported on by Electronics magazine as early as April 1984.

A five-chip set that may be the first Complementary-MOS implementation of a mainframe-class computer could show up in Sperry Corp. products next year. The Micro-1100 chip set will provide performance in the range of Sperry's 80 general-purpose mainframes. With as many as 200,000 transistors to a chip, the Integrated Circuits (IC) will be built with a process featuring 1.2-µm geometries and double level metal.

Other computer makers, including Digital Equipment Corporation (DEC), Data General, Hewlett-Packard, and NCR, are producing superminicomputers and mainframes or plan to do so, but the other designs are typically done in a more power-hungry n-channel MOS process.

The chip set is now entering the prototype stage at the Eagan, Minn., Semiconductor Operations plant described on p. 54." {Editor's note: p.54 wasn't available – see the Semiconductor Operations history starting on page 18 of http://vipclubmn.org/Articles/UnivacSemiconductorPaper.pdf.}

The Display Boards, thanks Carl.



The Lawshe Memorial Museum is at South St. Paul Minnesota.

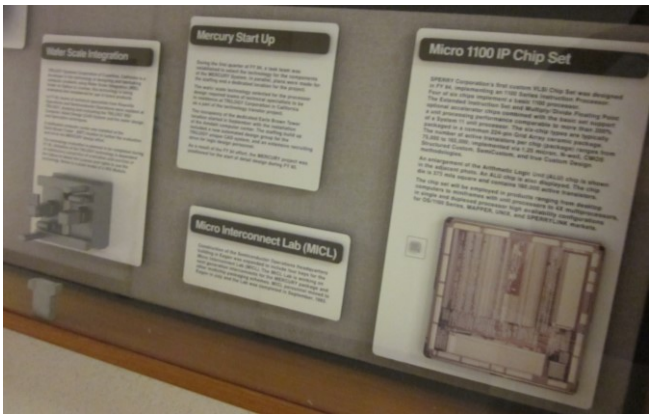
These are the first micro-1100 production wafers manufactured in Eagan, MN on August 1, 1985. {Editor's Note: Yes, the press reported five chips and six are shown here. A sixth floating point operations chip was added after the 'press info' was released.}

Time Line

January 1983	Project started
April 1984	Press article (leaked?)
August 1985	First Silicon wafers produced
1986 - prototype	Micro 1100 Chip Set was in the ORION1
1987	Burroughs/Unisys announce closing of Eagan chip manufacturing facility
1988	2200/400 began production line of chip use
1989?	Chips being manufactured at ?Intel?

[1]An extraction from page 27 of http://vipclubmn.org/Articles/univac2unisys.pdf:

MICRO-1100 IP CHIP SET - SPERRY Corporation's first custom VLSI Chip Set was designed in FY84, implementing an DIDI Series Instruction Processor. Four of six chips implement a basic TYDI processor. The Extended Instruction Set and Multiply/Divide Floating Point optional accelerator chips combined with the basic set support a unit processing performance comparable to more than 200% of a System-11 single unit processor.



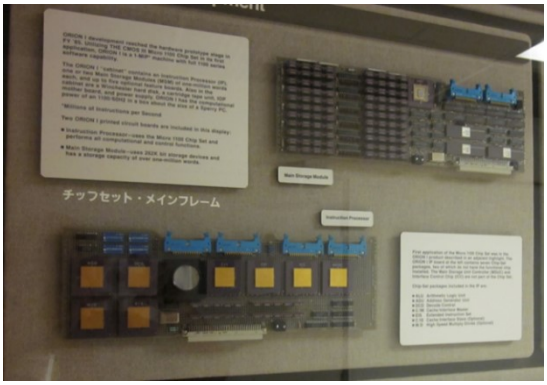
The six chip types are typically packaged in a common 224-pin Grid Array package. The number of active transistors per chip (package) ranges from 75,000 to 165,000: implemented via 1.25-micron N-well CMOS Structured Custom, Semi-Custom and true Custom Design.

An extraction from page 28/29 of http://vipclubmn.org/Articles/univac2unisys.pdf:

MICRO-1100 DEVELOPMENT - ORION 1 Development reached the hardware prototype stage in FY85, utilizing the CMOS 111 Micro 1100 Chip Set in its first application. ORION 1 is a 1-MIP (millions of instructions per second) machine with full 1100 series software capability. The ORION 1 "cabinet" contains an instruction processor (IP), one or two Main Storage Modules (MSM) of one million words each and up to five optional test feature boards. Also, in the cabinet is a Winchester hard disk, a cartridge tape unit, an IOP mother board, and power supply.

Orion 1 has the computational power of an 1100/60 H2 in box about the size of a Sperry PC. The instruction processor uses the Micro 1100 Chip Set and performs all computational and control functions. The Main Storage Module uses 262K bit storage devices and has a storage capacity of over 1 million words.

First application of the Micro-1100 Chip Set was in the ORION 1 product described in an adjacent highlight. The ORION 1 IP board at the left contains seven Chip-Set packages, two of which do not have the functional chip installed. The Main Storage Unit Controller (MSUC) and Interface Controller Chip (ICC) are not part of the Chipset. Chip-Set packages included in the IP are: Arithmetic Logic Unit (ALU), Address Generator Unit (AGU), Decode Control (DCD), Cache Interface Master (CIM), Extended Instruction Set (EIS), and the optional - Cache Interface Slave (CIS and High Speed Multiply /Divide (M/D).



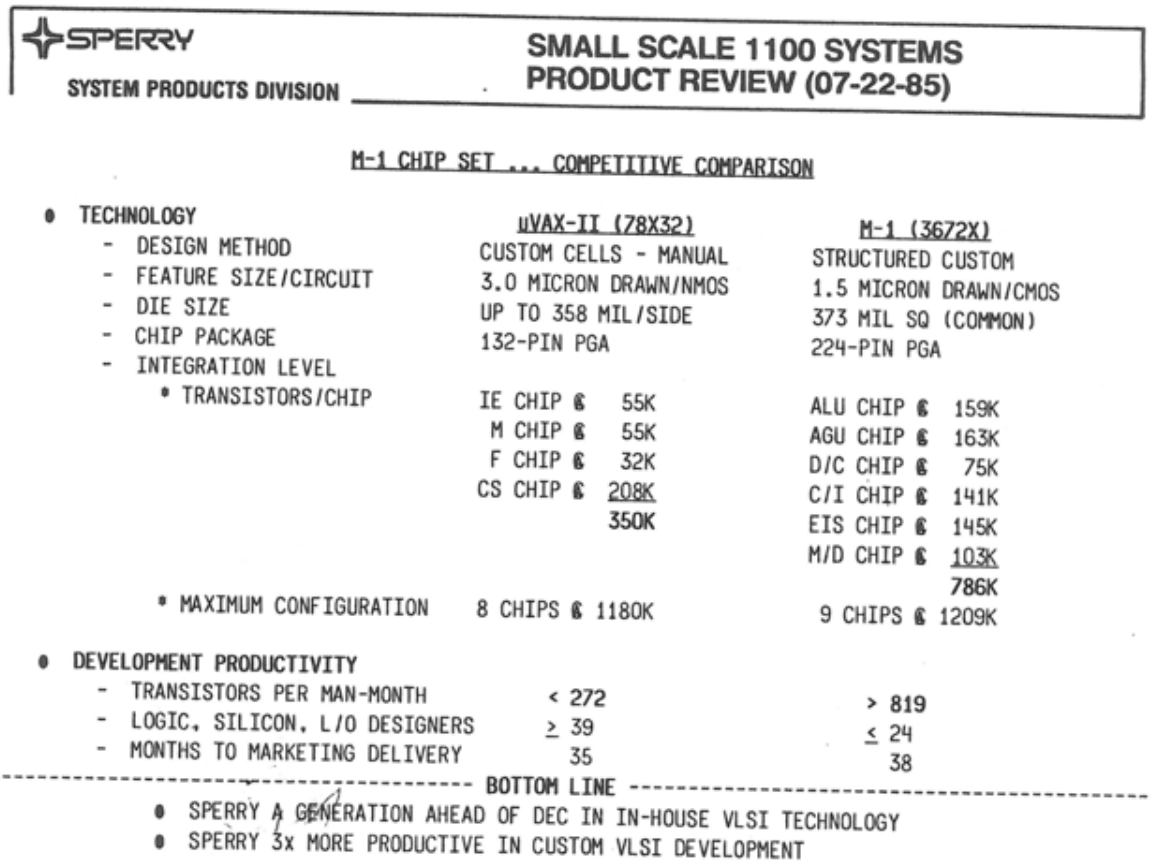
[1] The univac2unisys paper has text and photos from Mike Svendsen with editing by Lowell Benson.

Extracted from http://vipclubmn.org/Articles/ThroughTheAges.pdf
The UNISYS 2200 series used the chip sets:

- 2200/400 first delivered in 1988, over 900 units built
- 2200/600 first delivered in 1988
- 2200/100 first delivered in 1989

The Presentation Slides

This 1985 internal presentation slide compares the six chip IC set with available information about the VAX-II development.



SPERRY
SYSTEM PRODUCTS DIVISION

SMALL SCALE 1100 SYSTEMS PRODUCT REVIEW (07-22-85)

M-1 CHIP SET ... COMPETITIVE COMPARISON

	uVAX-II (78X32)	M-1 (3672X)
• TECHNOLOGY		
- DESIGN METHOD	CUSTOM CELLS - MANUAL	STRUCTURED CUSTOM
- FEATURE SIZE/CIRCUIT	3.0 MICRON DRAWN/NMOS	1.5 MICRON DRAWN/CMOS
- DIE SIZE	UP TO 358 MIL/SIDE	373 MIL SQ (COMMON)
- CHIP PACKAGE	132-PIN PGA	224-PIN PGA
- INTEGRATION LEVEL		
• TRANSISTORS/CHIP	IE CHIP @ 55K M CHIP @ 55K F CHIP @ 32K CS CHIP @ 208K 350K	ALU CHIP @ 159K AGU CHIP @ 163K D/C CHIP @ 75K C/I CHIP @ 141K EIS CHIP @ 145K M/D CHIP @ 103K 786K
• MAXIMUM CONFIGURATION	8 CHIPS @ 1180K	9 CHIPS @ 1209K
• DEVELOPMENT PRODUCTIVITY		
- TRANSISTORS PER MAN-MONTH	< 272	> 819
- LOGIC, SILICON, I/O DESIGNERS	≥ 39	≤ 24
- MONTHS TO MARKETING DELIVERY	35	38

BOTTOM LINE

- SPERRY A GENERATION AHEAD OF DEC IN IN-HOUSE VLSI TECHNOLOGY
- SPERRY 3x MORE PRODUCTIVE IN CUSTOM VLSI DEVELOPMENT

{Editor's note/opinion: The Sperry philosophy was to innovate and develop the technologies to keep them ahead of other computer companies – the VAX was a Digital Equipment Corporation product. The philosophy changed to buy technology after Burroughs bought Sperry to form Unisys. Thus, instead of leading the corporation morphed into a follower behind other companies.}

SPERRY
SYSTEM PRODUCTS DIVISION

SMALL SCALE 1100 SYSTEMS PRODUCT REVIEW (07-22-85)

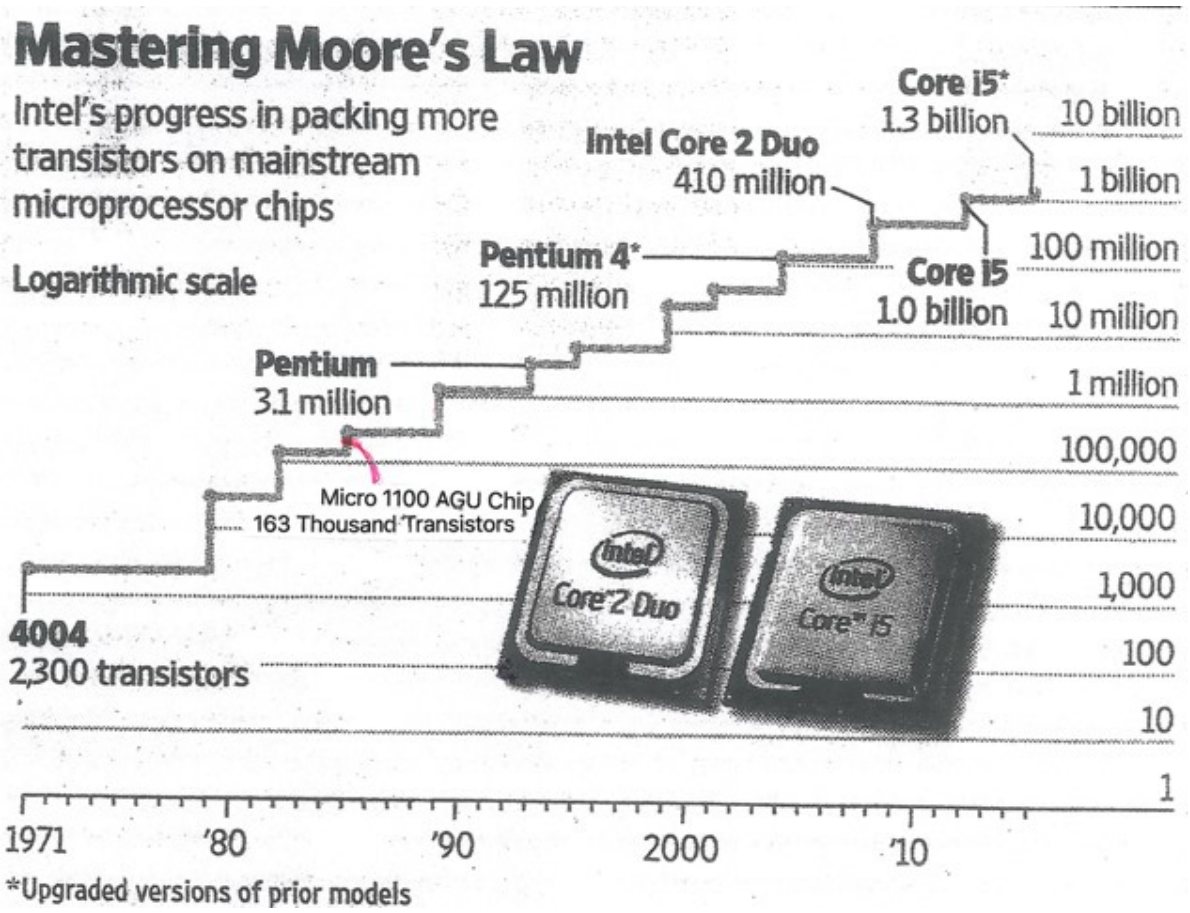
M-1 CHIP SET ... COMPETITIVE COMPARISON

CHARACTERISTICS	μVAX-II (78X32)	M-1 (3672X)
MACHINE MODES	VAX	BASIC AND EXTENDED
# INSTRUCTIONS, IN H/W IN S/W	245 59	504 0
EXTERNAL/INTERNAL DATA PATHS	32/32 BIT	36/72 BIT
GENERAL REGISTER STACK	16W	128W
IP CACHE, MAXIMUM SIZE HIT RATE	2KW 90% @ 2KW	16KW 90.5-98.5% @ 8KW
CYCLE TIMES	200 NS	80 AND 108 NS
BOTTOM LINE	VLSI MINI 80% OF 11/780* VMS SUBSET	VLSI MAINFRAME 100 TO 162% 1100/61H FULL OS/1100

*BENCHMARKS AT CARNEGIE-MELLON RAN 70% TO 90%

{Editor's note: It was quite appropriate to compare performance with the VAX-II. Note that the chip set has 504 instructions implemented with hardware whereas the VAX has some functions performed with software. These are likely floating-point operations for much of the higher-level mathematics.}

Moore's Law - the principle that the speed and capability of computers can be expected to double every two years, as a result of increases in the number of transistors a microchip can contain.



{Note that this Moore's Law image was originally copied from the Wall Street Journal.}

{Editor's Notes: This chart shows where the Micro 1100 chip set fits on the Moore's Law scale. In the early 70s Intel had the 4004, a microprocessor on a chip with 2,300 transistors. Then they had the 8080 8-bit microprocessor on a single chip. Lowell's home PC being used with Microsoft Word to generate this paper has the Intel Pentium I-5 for a processor, laptop has an I-7.}

Biographical Notes

Carl A. Johnson graduated with honors from the University of Minnesota's Institute of Technology with a Bachelor of Science degree in electrical engineering in 1955, following an 18-month program in electronics at Dunwoody Industrial Institute. Johnson also completed numerous post-graduate courses with Sperry and the University of Minnesota in management, strategic planning, communications, team development, and quality.

He started his career with Engineering Research Associates in 1954 and retired from UNISYS in 1986 after 32 years of technical and managerial experience in computer systems, circuits and packaging, semiconductor devices, memory storage equipment, business and product strategy, program management, acquisition and competitive analysis and communications product development.

Mike Svendsen graduated in 1959 from the University of Minnesota with a Bachelor of Science degree in Electrical Engineering. I had asked my uncle (Commander Edward C. Svendsen) if he had any thoughts about the electronics industry and where I might go to work. His comment was brief: "well, UNIVAC is doing some interesting things with computers". UNIVAC was close to home, so I joined in Aug '59. The semiconductor industry was in its infancy then; the majority of my 25 years at Univac were involved in semiconductor specification, design, evaluation, testing, quality, failures, cost, availability and manufacturing at our suppliers and at our in-house facility. You might say we matured together.

I worked at all the plants in the Twin Cities and in many disciplines: Electrical Engineering, Reliability, Test, Procurement, Quality, Production, Quality Assurance, Operations Management, Bipolar Operations and the Semiconductor Control Facility. I was a member on Sperry's Corporate Councils on Semiconductors, Standardization, and Procurement.

Lowell Benson graduated in 1966 from the University of Minnesota with a Bachelor of Electrical Engineering degree. He had a wide variety of positions during his UNIVAC 1960 to UNISYS 1994, 33.5 year career, http://vipclubmn.org/PeopleDocImg/Vol01Book1.pdf.

Lowell chaired the VIP Club's Legacy committee from October 2005 through December 2019. As such, he developed the Club's IT Legacy Anthology and has edited all the 150+ papers for the Our Stories website chapter