Engineering Achievement Award

Introduction

This paper is a recap of queries and responses the Legacy Committee sought to identify the background which led to a plaque commemorating the 200 Nanosecond Memory award shown below.

E-mail from Quint Heckert to Larry, Lowell, and Harvey dated April 1, 2010: "This is a scan of a photo I found in some of the files we received for our Legacy Committee. Thought you might want to add it to the significant events table and possible put a copy of it on the web."

Question

Larry Bolton: "Do we know any more about this 200 ns memory? What technology was involved - core or film? Or even semiconductor?"

Investigation Communications

Quint: "This is all I've seen. Could it be related to or be the NIKE-X memory photos we found on Monday? When was NIKE –X?"

Larry: "Nike-X was about that time. However, there is some question about how much of the design we did. We have a whole series of aperture cards in the vault which indicates that we took another design and put our part numbers on it to manufacture it. It looks like most was designed by someone else (AT&T, Western Electric, etc.). Some of the design features are not those we typically used. This does not mean we did not design all or part of the memory however.

Lowell to John Alton, Dick Erdrich, Gary Hokenson, Ernie Lantto, Don Mager, and Dick Petschauer: "Do you recall who might have been working on memory development the year before or during 1966? Was this thin film memory or mated film memory or plated wire memory? I think that this was a couple of years before the 16 bit memory chip (semi-conductor) was used for the AYK-10. Do you have any idea which project this was for?

Dick Erdrich: "All, the 16-bit memory cell was chosen for use in the CP-890 design over a film memory sometime in 1966 by Don Mager. As I remember, he had to jump through the usual number of hoops to get management to agree. He was aware of what the Plant 1 film memory group was doing at the time and could probably determine whether this was their award or not. The other name I remember is Ken Hogenson who was one of our (Plant 5 engineering) contacts with the film memory group."

Gary Hokenson: "The memory might have been Nike-X or S-3A mated film. Jim Bratsch was the mechanical and he might remember."

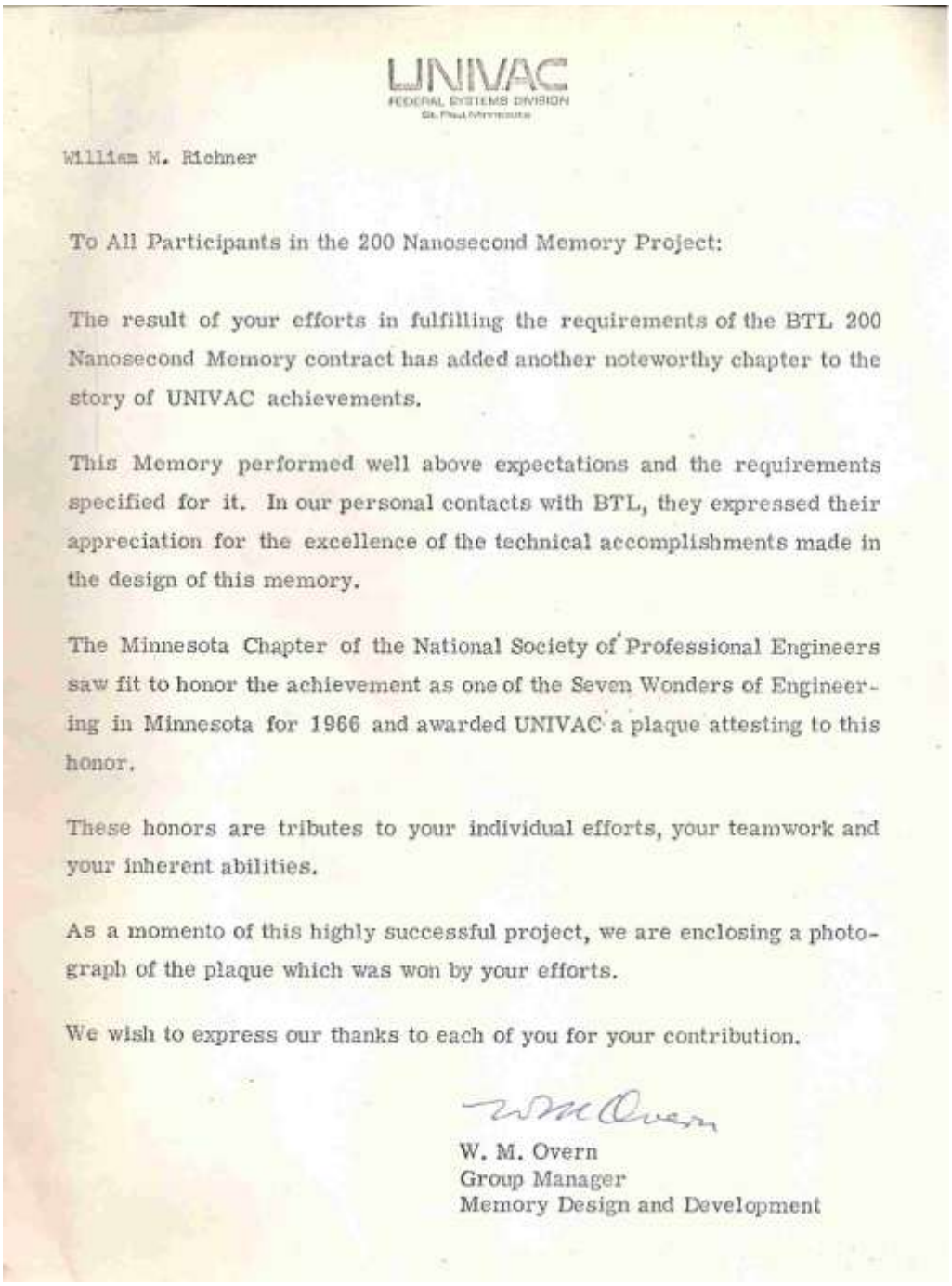
Don Mager: "I would guess that the film memory referenced was the one we used for control memory in the 1230 computer (sometimes called Modified 20B) we developed in 1965 for the NASA Apollo tracking sites. We planned to also use it for control memory in the CP-890 Poseidon Navigation Computer, but part way into the design switched to the 16-bit Integrated Circuit which was just becoming available. In circa 1970 we used mated film for the main memory in the S3-A computer."

John Alton: "I believe that Bill Overn and Bob Boylan were working in the memory development group in the1966 time period. I can't provide any clues as to their whereabouts. I support Don Mager's suggestion that this award probably refer to the mated film memory, but I can't remember enough to confirm the 200 ns speed."

Ernie Lantto: "I do not remember this award."

Dick Petschauer: "I was away from the company at the time, so I can't help. But I am quite sure that it was not a commercial product."

Quint: "All; William N. Richner was one of the members of the team. I just found a memo yesterday (copied hereunder) and am sending him an e-mail to get information on this.



UNIVAC
FEDERAL SYSTEMS DIVISION
Sp. Paul Minnesota

William N. Richner

To All Participants in the 200 Nanosecond Memory Project:

The result of your efforts in fulfilling the requirements of the BTL 200 Nanosecond Memory contract has added another noteworthy chapter to the story of UNIVAC achievements.

This Memory performed well above expectations and the requirements specified for it. In our personal contacts with BTL, they expressed their appreciation for the excellence of the technical accomplishments made in the design of this memory.

The Minnesota Chapter of the National Society of Professional Engineers saw fit to honor the achievement as one of the Seven Wonders of Engineering in Minnesota for 1966 and awarded UNIVAC a plaque attesting to this honor.

These honors are tributes to your individual efforts, your teamwork and your inherent abilities.

As a momento of this highly successful project, we are enclosing a photograph of the plaque which was won by your efforts.

We wish to express our thanks to each of you for your contribution.

W. M. Overn
Group Manager
Memory Design and Development

Quint to Mr. Richner: "Mr. Richner; As a member of the UNIVAC legacy committee I am requesting your assistance to clear up some questions relative to a 200 Nanosecond memory that was developed in the 1966 time frame. Last week I found a photo of a plaque that was presented to UNIVAC by the Minnesota Chapter of the National Society of Professional Engineer for a 200 Nanosecond Memory and naming it one of the Seven Wonders of Engineering. We have trying to determine what project this memory was used on and what the technology was. Yesterday while going through some other documents I found a copy of the memo from W. M. Overn to you relative to this memory and the award. The memo states that BTL expressed their appreciation for the excellence of the accomplishment. I assume this is a reference to the old Bell Telephone Labs and that the program was NIKE-X. Would you please verify the above assumptions or correct them and we'd be very appreciative if you could give us more detail on this memory."

Mr. Richner: "Hi Quintin: You are correct in that it was for the Nike-X program with Bell Labs. The details of the technology are getting dim in my memory. My group was responsible for the packaging; therefore, I was not that close to the technology. It was called the "twister" memory which was wires twisted around an iron core. I can't think of any of the memory design people who are still around. If I think of someone I will let you know. Sorry that I can't provide more info."

Quint: "I just spoke with Tom Mack, who was the Engineering Manager on the 200 Nanosecond Memory project. The memory was built for BTL for use on NIKE-X and was a thin film, planar film, glass substrate, 3mil. Tom says the device we built, he believes, was a prototype and that we used all BTL transistors. The contract was highly incentivized and the specifications did not allow any bad cells in the memory. The test was passed and UNIVAC collected the incentive fee. The only failure during the test was a BTL supplied transistor. The engineering supervisors working for Tom at that time were Alex Trembley, film stack, and Ken Pearson, who had responsibility for the circuitry."

Ken Pearson – reply 2: "The 200 Nanosecond Main Frame Memory was for the upgrade of the Nike Zeus System I described and was for the next generation Nike X Computer System which replaced the original Twistor Film Memory with the 200 Nanosecond Flat Film Memory. That Computer System was deployed on the Kwajalein Islands in the Pacific, and I did not go into the field with that System – please update my first reply."

Ken Pearson – reply 1: "Hi Lowell, Yes! I remember the 200 nsec memory very well as Sam Meddaugh and I co-authored a paper about it entitled "A 200 Nanosecond Main Frame Memory" and presented it at the 1965 IEEE Fall Joint Computer Conference in San Francisco. It was the Mainframe Memory for the Nike-X Anti-Missile Project Computer and was deployed on the Kwajalein Islands in the Pacific. It was the replacement for the Nike- Zeus Anti-Missile Missile Project Computer and the first one was installed at the White Sands Missile Range. I spent several weeks on-site at the Missile Range working on the computer to make sure everything was working properly. I was at the site during a test firing in which an ICBM Missile was fired from Vandenberg Air Force Base in California and successfully intercepted by the Nike Zeus Missile over New Mexico. It was spectacular to see the white missile streaks in the blue sky cross paths in the sky. A successful interception was a given proximity to the target as the Nike Zeus Missile had

explosives which would destroy the target Missile. One of my favorite memories of a great work career - I hope this information helps the questions. Thanks, Ken Pearson

Don Mager – second response: "A bit more background: The 1230 computer project was at Plant 5 and Curt Hogenson was the key engineer and representative from the Plant 1 memory group. A 400 nsec mated film memory was used for the control memory to store index registers, buffer words, etc. The 1230 computer Serial #1 was shipped to NASA Goddard August 1965. I'm quite familiar with this project because I was the Project Engineer and also designed the control section which utilized the 400 nanosecond film memory."

{Editor's note: *The clip below was the April 2007 Legacy website 'Article for the Month'*.}

New Computer System Now Being Installed in Apollo Network

A new computer system of vastly increased capabilities, designed expressly for the Apollo program, has arrived at Goddard from Univac Military Systems Division in St. Paul, Minnesota, and is being implemented into the Manned Space Flight Network, reports Dale W. Call, Head of the Manned Flight Engineering Branch.

The Apollo computing system, consisting of two Univac 642B Mod. computers and peripheral equipment, are identical in every respect with exception to the mission requirements which are assigned to them.

One computer system will be assigned the task of processing all telemetry data for display at the Flight Control Consoles to be presented on cathode ray tubes, transmission of data via high speed (2.4 kbs) data lines, and transmission of 60 wpm, 100 wpm teletype messages to the Mission Control Center in Houston, and other remote sites.

The second computer will be assigned the task of command data processing between the orbiting spacecraft and the Mission Control Center. The computer under program control will receive command information from the Mission Control Center via high speed data lines and store this data in memory until required for retransmission to the orbiting spacecraft at acquisition. This command can be changed manually by the Flight Controller located at the consoles, or can be changed in the computer by additional transmission of data from the Mission Control Center in Houston.

In addition to the functions previously described, each computer will have the capability of supporting the other by performing both tasks should a failure in either computer occur at any time during the mission.

Eventually a total of 39 computer systems will be installed throughout the Apollo network: Apollo ships; Carnarvon and Canberra, Australia; Bermuda; Guam; Guaymas, Mexico; Merritt Island, Florida; Ascension Island (in the Atlantic, off African coast); Kauai, Hawaii; Madrid, Spain; Goldstone, California; Corpus Christi, Texas; Antigua Island and Grand Bahama Island in British West Indies; and Grand Canary Island (off the African west coast). Manned Spacecraft Center, Houston, will also receive computer systems for simulation and checkout purposes.

***DON MAGER** and Ed Willis (foreground) inspect a chassis that has been removed from the 642B Modified Computer. In the background are Les Brunker, Program Manager, and Glen Johnson inspecting a partially removed chassis from the computer.*

Lowell Benson to Curt Hogenson: "Curt: Your name was noted by Don Mager and Dick Erdrich as our Legacy Committee has been pursuing information about a 1965/66 200 Nanosecond Memory. I'm attaching some notes to date about the investigation. We'd appreciate any comments which you may have about the project. Thanks,"

Curt Hogenson: "Lowell: I was involved with this 200 Nsec Memory project (BTL/Nike-X) in the early stages when the Memory Design and Development Department was still staffing up for this effort. I believe this was in late 1964. I had responsibility for the test equipment. Steve Tako took over when I was reassigned to the 1230 Project. He reported to Tom Mack.

I'll try to add some clarity to the discussion regarding the 1230 Film Memory and "mated film". The 1230 Film Control Memory was the first production memory to have the bit/sense lines vacuum deposited with (mated with) the memory elements in between. This was a 400 nsec memory. I believe the term "mated film memory" was used later on, probably when the "solid stack" main memory was designed by Roy Prohofsky's group for use in the UYK-7 computer.

I was also involved with redesigning the 1230 control memory to use the 16 bit memory chip which was mentioned. The chip memory was used as the replacement choice when the need arose.

I've included PDF scans of the front page of June/July 1965 issue of the Univac News which I saved. The article on the 1230 film memory has more information, names and pictures of the people who attended the presentation in Plant 1. I also have JPEG scans of this page at 3X the file size if you need them.

On a personal note, on the back page of this 1965 issue you and I are listed along with over 200 others who had 5 year anniversaries in June or July.

I enjoyed the 1230 project very much and my short stint on the Nike project. I also enjoyed responding to your request. Thanks for asking! Curt Hogenson

RE-TYPE of the 1965 Univac News article: "A new Univac control Memory which represents a major technological advancement in memory development was demonstrated for a group of Defense Systems Division executives in Plant 1 this month. The development was called "another Univac first" by Memory Engineering Manager Bill Overn, whose department was responsible for the design of the new element.

"The improved memory, which utilizes a new type of thin-film element, is faster, more reliable, easier to maintain and more resistant to temperature variations than other types of memories, such as core memories", Overn said.

The main innovation of this development is the technique of vacuum depositing some of the required conductors as well as the memory elements.

In previously used planar film processes, only the metallic film elements were deposited and all the conductors were separately fabricated and then added to the substrate as overlays. The new technique makes possible the batch processing of some of the wiring as well as the memory elements.

now an additional 182,640 for a total of 385,640 square feet, to become the Space Center's largest tenant.

wing to its headquarters in Plant 1, and the acquisition of 11,000 square feet of existing floor space at Plant 3.

CONTROL MEMORY demonstration is conducted by Curt Hogenson, pointing, right, who explains the innovations of the improved memory to R. E. McDonald. At left is W. J. Malloy, group manager, Advanced Development. In background, left to right are O. C. Bixler, G. M. Bestler, L. W. Reid, V. E. Leas, R. R. Coon, A. J. Hyman, G. G. Probst, and R. E. Hegler.

TEAM THAT PARTICIPATED in development of the new Control Memory, from left front: Project Engineer Curt Hogenson, Bill Malloy, Ted Maki, Howard Silver, Chuck McKee and John Lundquist. Rear: Tom Peckham, Dean Morgan, Bill Overn, Ralph Oliver and Bob Boylan. Not pictured is Bob Bergman.

The first production model of the new Control Memory is used in a new computer now under development. "The new Control Memory, with a 400-nanosecond cycle time, has either 128 or 256 30-bit words. It has wider operating margins, a simpler design and lower cost than previously used film or core memories", Overn said.

The same memory can be expanded from four to eight thousand words for operation at 500 nanoseconds. It also can be used as a 200-nanosecond control memory of 128 to 256 words, using faster electronics which are available today. Future memories, Overn added, will have wider applications – "ranging from ultra-high-speed memories with 20- to 40 nanosecond cycle times, to vary large main frame memories with 500 nanosecond cycle times or less. "

The cost of the new film memories will be competitive with core memories of the same size, and the memory will be about four times as fast as core memories in the same cost bracket. This cost will be further reduced, Overn said, by 'batch processing' of the memory sub-assemblies. They will be produced in a new vacuum lab presently being prepared in Plant 1.

During the recent demonstration, the Serial 1 production model memory was praised by R.E. McDonald, vice president and general manager of the Defense Systems Division, as a dramatic demonstration of what Univac creativity can do in advancing the state of the art. "It's a tremendous job . . . well done."

A major factor in the success of the memory development, Overn said, was the high caliber of technical competence, enthusiasm and cooperation of the engineering and manufacturing groups involved in the project.

"The memory was developed in less than six months – a real tribute to the team that designed and buil it. An achievement of this scope obviously reflects the contributions of many persons, but special acknowledgment is due the engineering – manufacturing team headed by Project Engineer Curt Hogenson." Others who participated in the development group were Ken Mulholland, Bob Bergman, Bob Boylan, John Lundquist, Ted Maki, Chuck McKee, Dean Morgan, Ralph Oliver, Tom Peckham and Howard Silver. "

End of newspaper article

What is a 'Control Memory'?

For the benefit of readers who haven't worked with computer architectures, it is appropriate to provide a high-level tutorial. A control memory was part of the Input Output Control (IOC) logic of a computer. Computers without a control memory, such as the AN/USQ-17, AN/USQ-20 and CP-901, used pre-allocated main memory addresses to retain I/O buffer control words – buffer end address in the upper half, start then current address in the lower half. There were 16 address cells for input buffers, 16 cells for output buffers, and 16 cells for multi-word external functions [command codes sent to magnetic tape units or display units or other complex peripherals.] When a peripheral was ready to accept a data word, the I/O control would fetch the buffer control word, use the lower half to fetch the data word, send it to the peripheral, increment the buffer lower half word then store it back into the allocated memory. After the increment, if the lower half was greater than the upper half – the buffer was completed so the IOC would notify the processor that the specified number of words had been transferred. Thus for each word transferred three main memory cycles were used – sometimes called cycle stealing – for each word transferred. So a computer like the CP-901 with a two microsecond main memory could transfer one word every six microseconds for a maximum transfer rate of 167,000 words per second.

In a computer with a control memory for the buffer control words, only the fetch or store of a transferred word accessed the main memory. Thus the 1230, with a two microsecond main memory, could transfer a word every cycle for a maximum transfer rate of 500,000 words per second.

In addition to buffer control words, some computers used control memory index registers, real time clocks, count-down clocks, etc. The second performance factor benefit of a control memory is that buffer control word processing didn't take memory cycles away from instruction and operand fetches so programs would be executed at almost the same speed whether I/O was transferring data or not.

Summary

Thanks to each of the query respondents who related his participation recollections of the 200 Nanosecond Memory development and the multiple product applications of the film memory technologies. The Legacy Committee welcomes other project stories related to memory development.