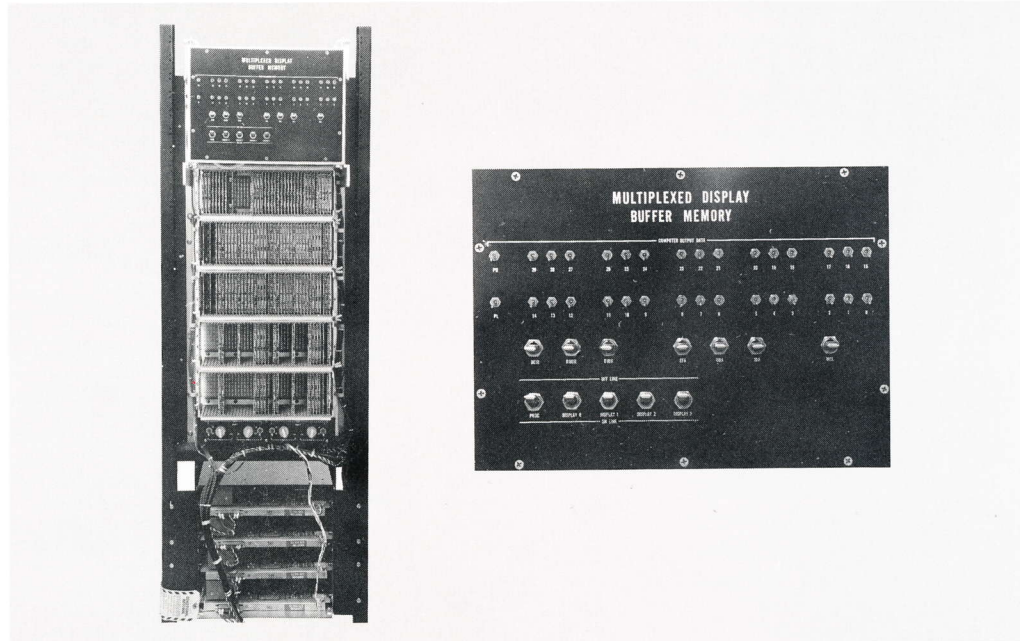


Multiplexed Display Buffer Memory (MDBM)

FA-8312

UNISYS



- Multiplexes one Input Output Processor (IOP) I/O channel to four displays
- Provides separate refresh display buffer memories (DBM) for up to four ARTS displays
- Dual channel IOP interface for failsafe/failsoft operation
- Semiconductor LSI memory, 1024 32-bit words/module
- Memory expandable from 1024 to 4096 words per DBM
- Reduces I/O channel requirements
- Frees IOP memory for other functions
- Provides refresh to displays during DPS failure
- Refreshes an ARTS display at maximum display request rate

Features

Multiplexed Display Buffer Memory

- Mounts in and occupies one fourth of a Processor Cabinet (PCAB FA-8301)
- Provides separate buffer memory for each display
- Plug-in semiconductor LSI memory
 - 1024 to 4096 words of 32-bit memory per Display Buffer Module in increments of 1024 words
 - Memory speed - 1.4 usec (maximum)
- Memory responds to External Function Commands from processors
- Maintenance panel services both dual channel multiplexers
- Capability to remove displays to an off-line condition through the maintenance panel
- Processor interface is dual channel, 32-bit, parallel, Type A (Unisys specification SB 10205)

Applications

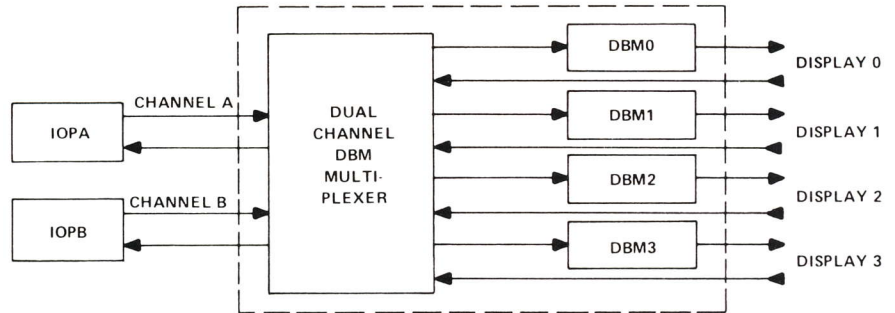
- Air Traffic Control
- On-line information storage and retrieval systems

Configuration Options

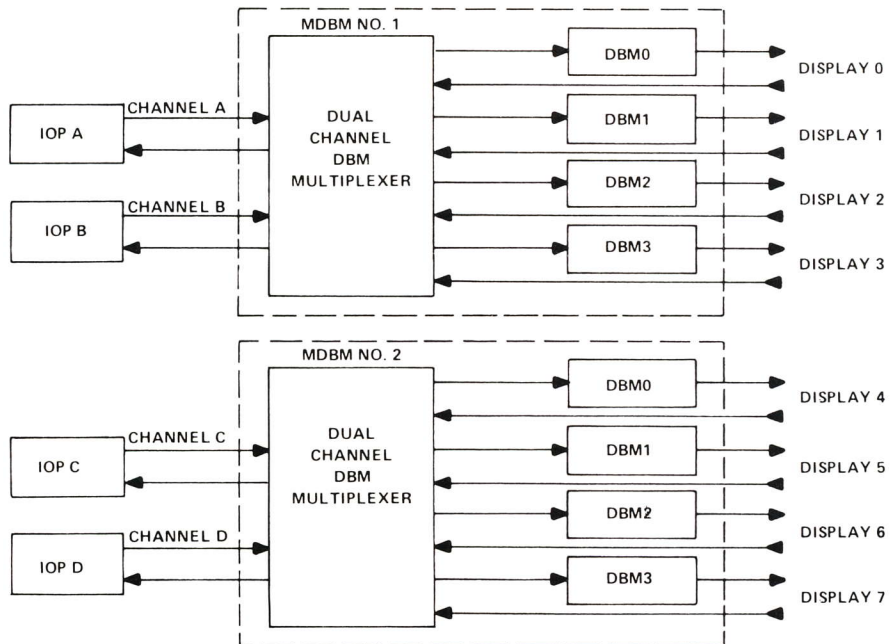
- Two dual channel DBM multiplexers can be mounted in one fourth of a PCAB (FA-8301)
- One to four DBM's per DBM multiplexer
- 1K to 4K of memory per DBM in 1K increments

Physical

- Power:
 - 120 VAC, 60 Hz, single phase
 - 152 watts (maximum)
- Operating temperature:
 - 15°C to 32°C (60°F to 90°F)
- Relative humidity: up to 80%



4 DBM MDBM Configuration



8 DBM MDBM Configuration

For additional information, write to
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